Life on the Edge

A Universal Grammar of Class D Amplification

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Definition

A class D amplifier is a power amplifier where all active devices in the power stage are operating in on/off mode.

- On=current, but no voltage
- Off=voltage, but no current

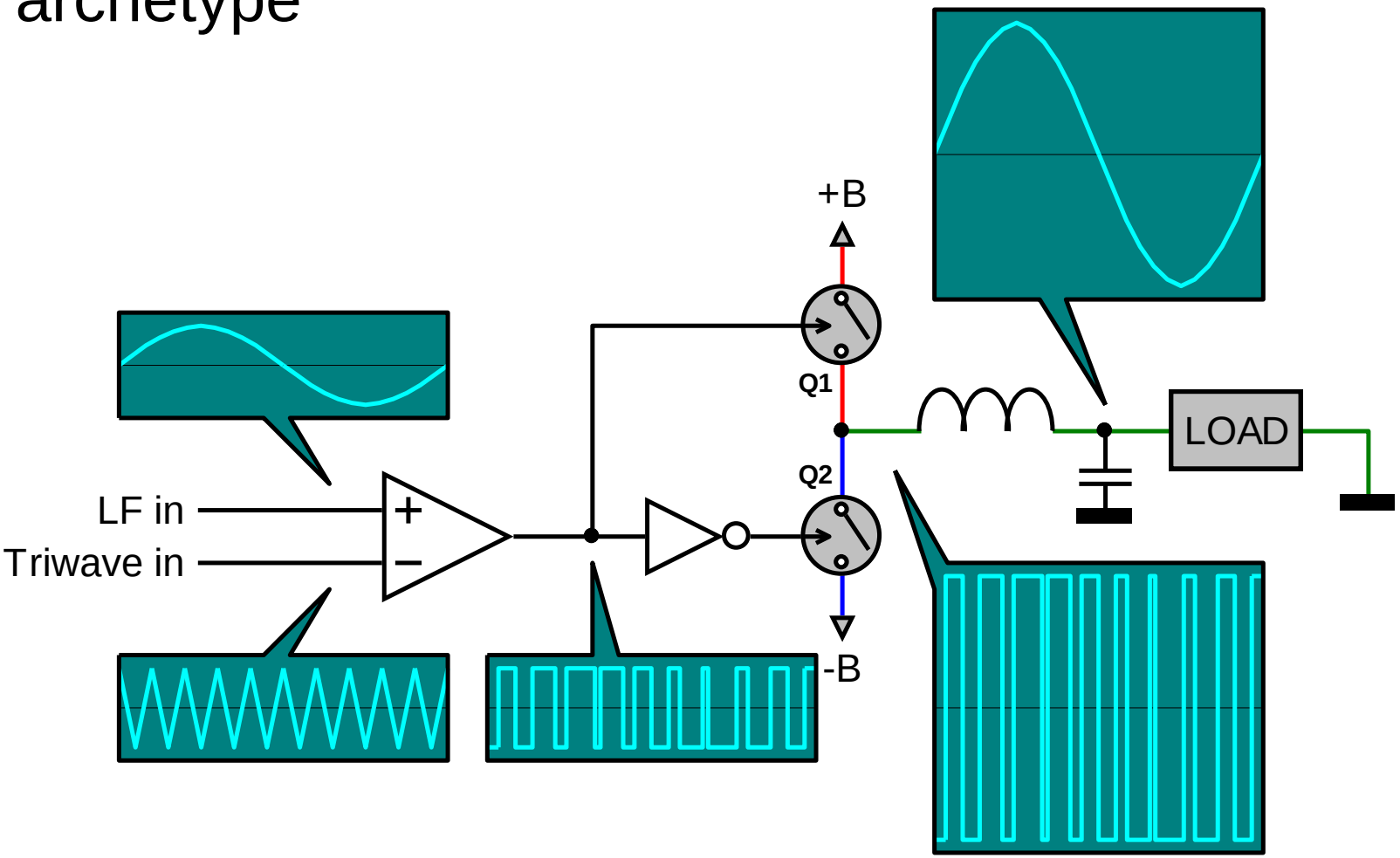
Definition

"Digital amplifier" is an oxymoron

- Voltage, current and time are physical quantities (analogue).
- Digital is strings of numbers.
- Speakers don't understand numbers.
- Class D requires analogue design skills to make work.
- DSP control may help solve or exacerbate analogue issues.

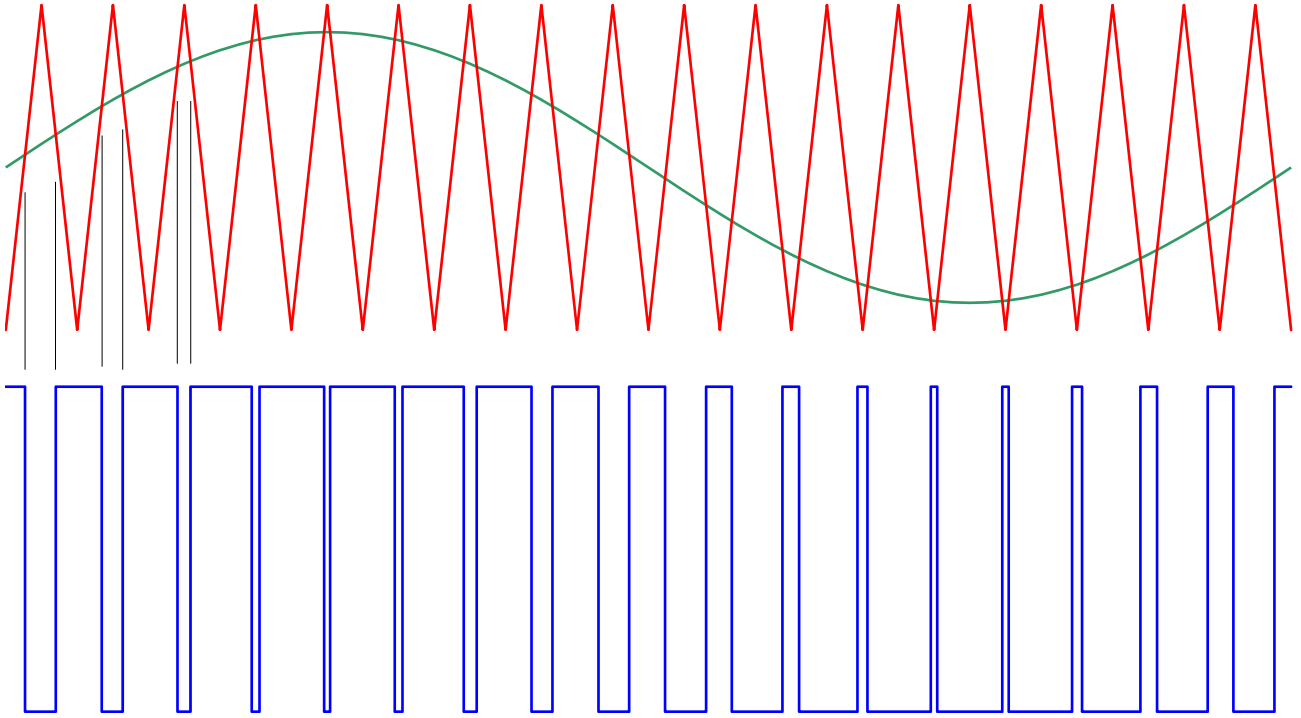
PWM basics

The archetype



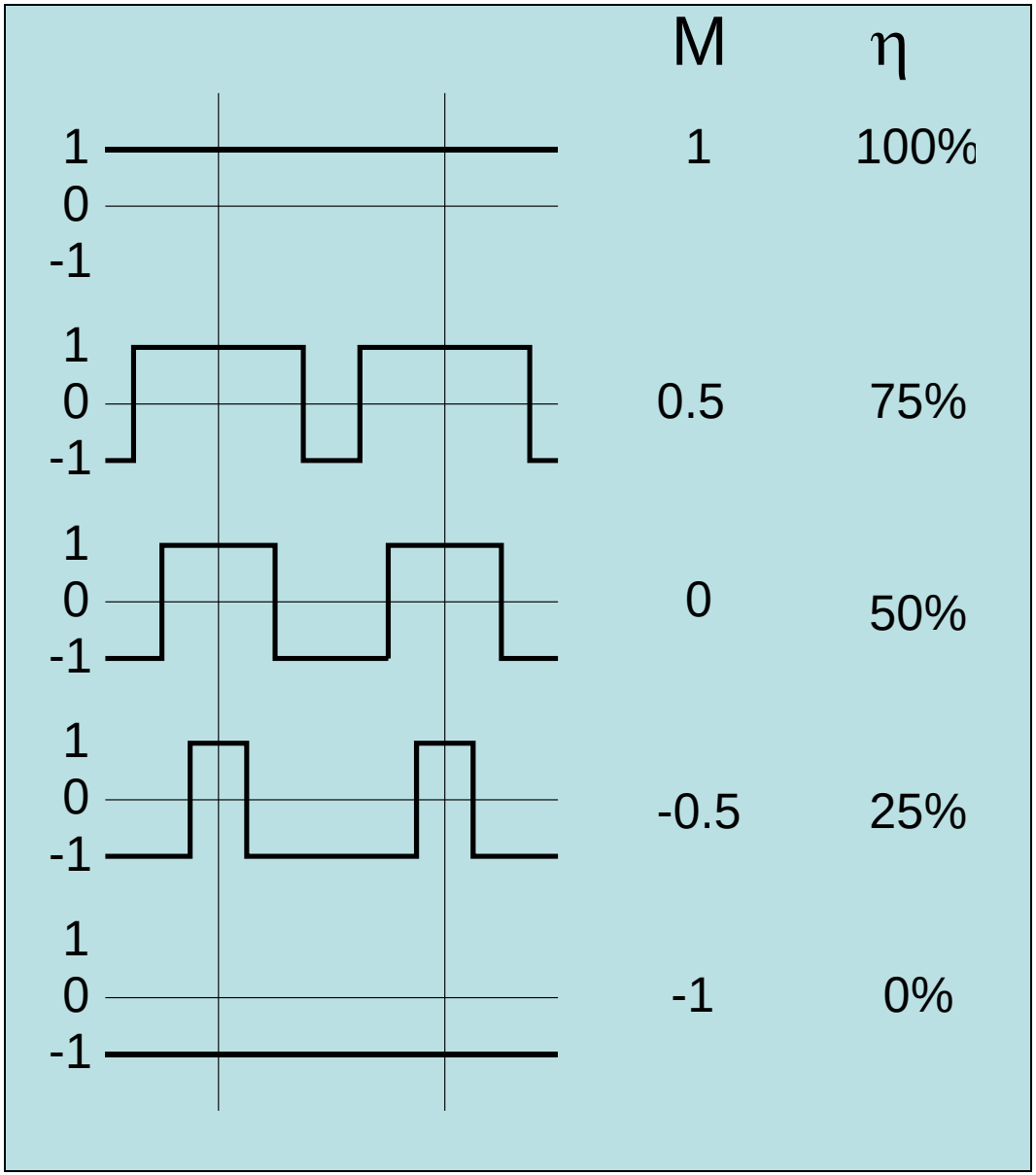
PWM basics

Two-state clocked PWM



$$A_V = \frac{V_{PWM,pp}}{V_{tri,pp}} = \frac{V_B - V_{-B}}{V_{tri,pp}}$$

Some conventions



$$t_{sw} = t_{on} + t_{off} = \frac{1}{f_s}$$

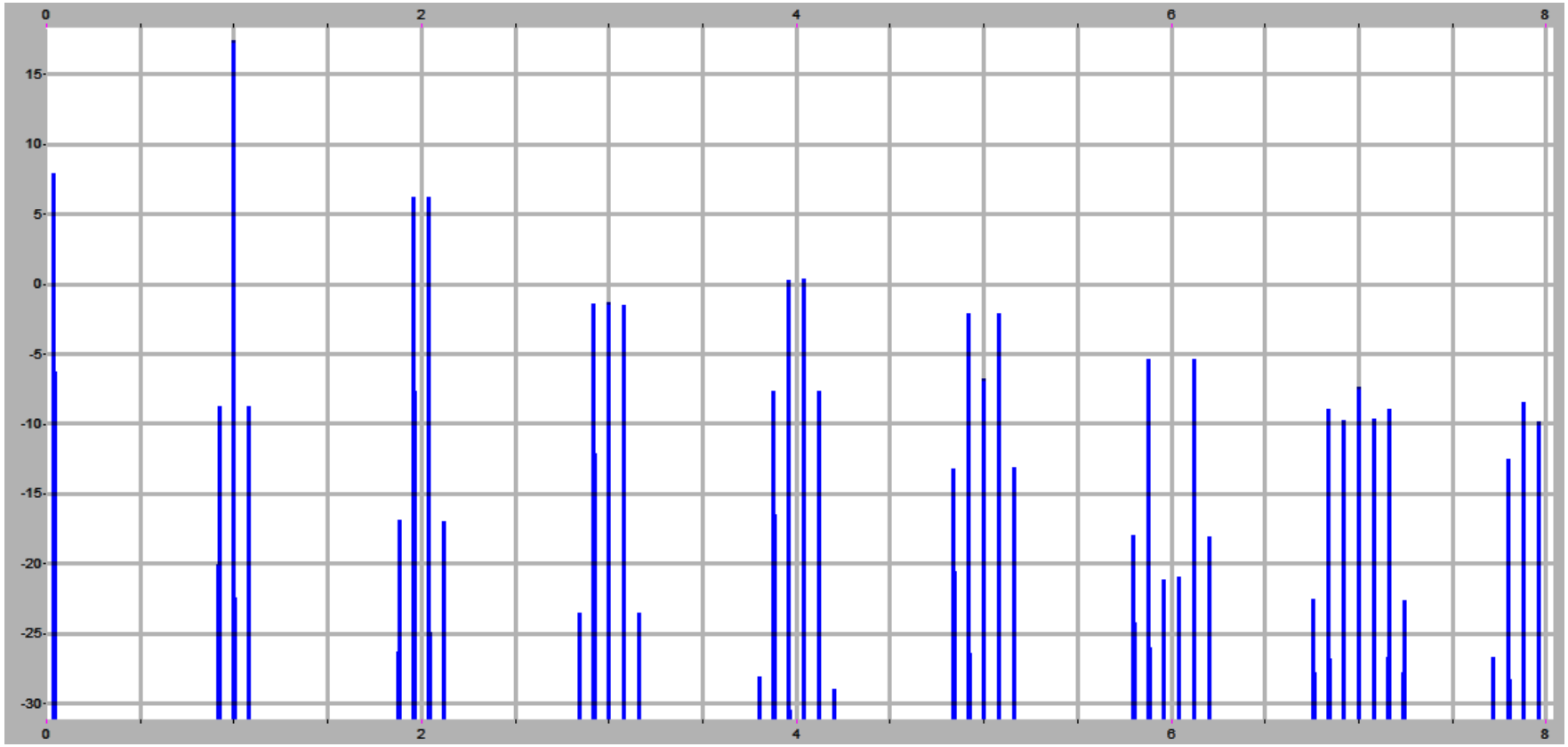
$$M = \frac{t_{on} - t_{off}}{t_{sw}}$$

$$\eta = \frac{t_{on}}{t_{sw}} \cdot 100\%$$

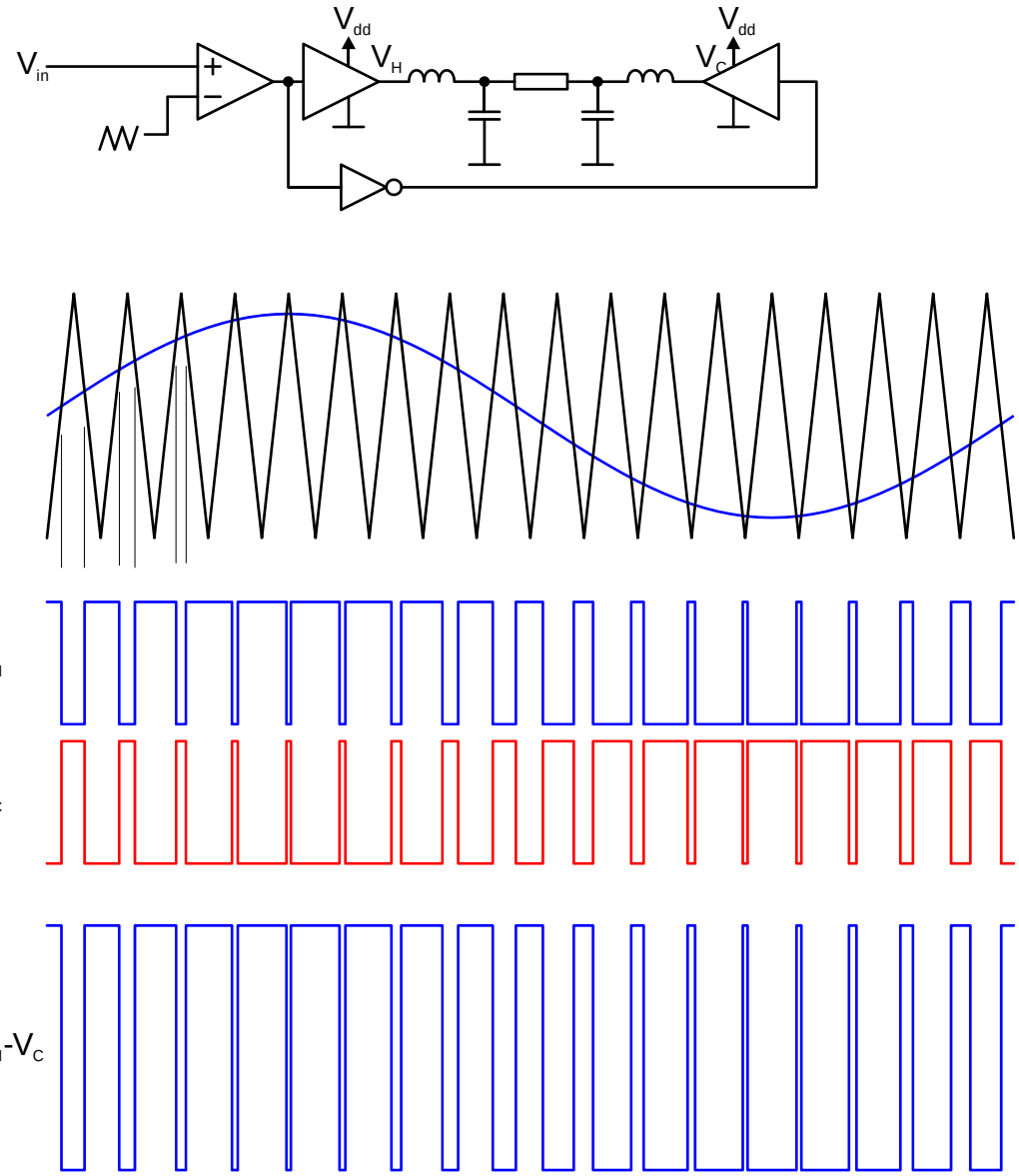
$$\Downarrow$$

$$M = 2 \cdot \eta - 1$$

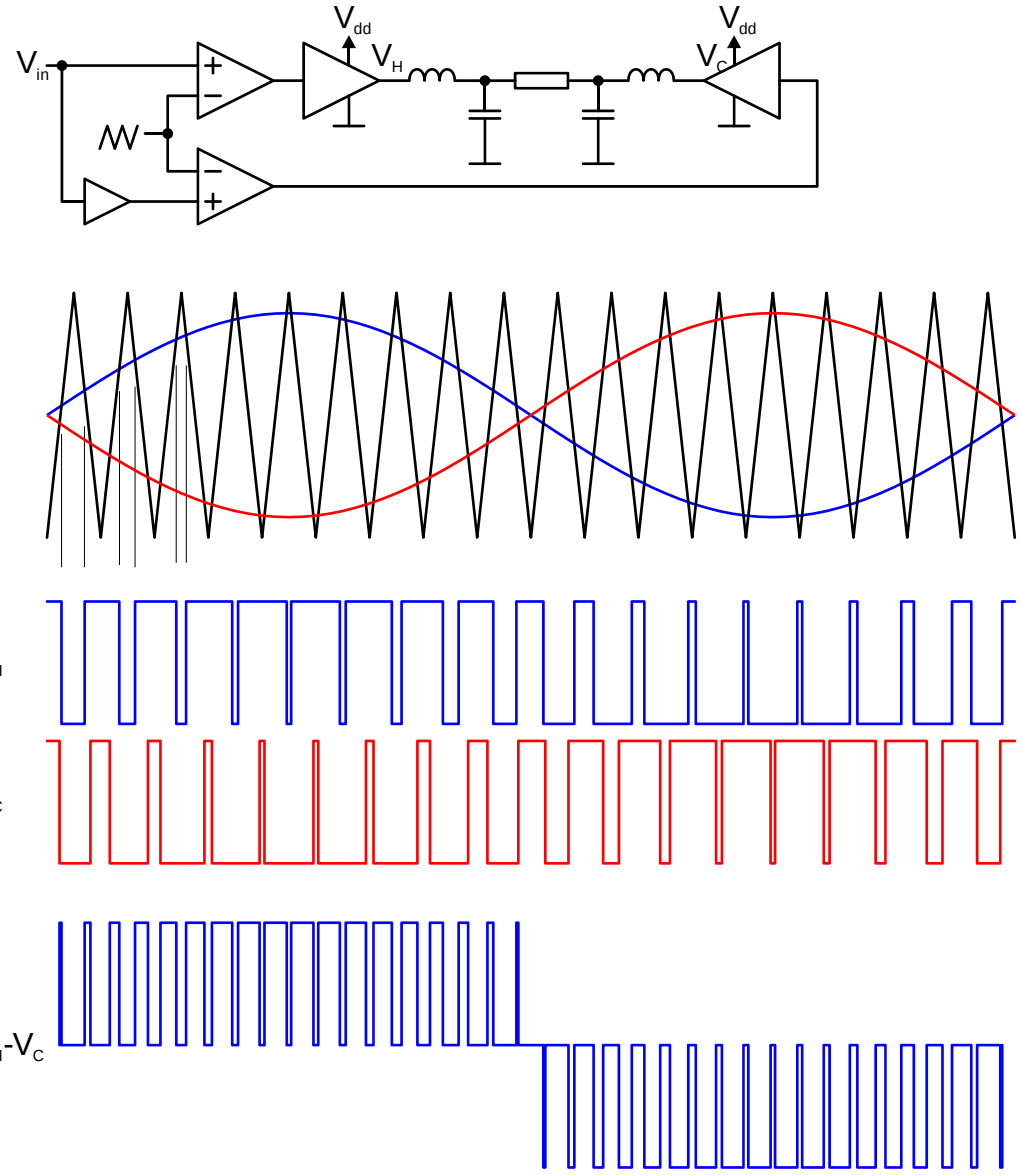
Spectrum of 2-state PWM



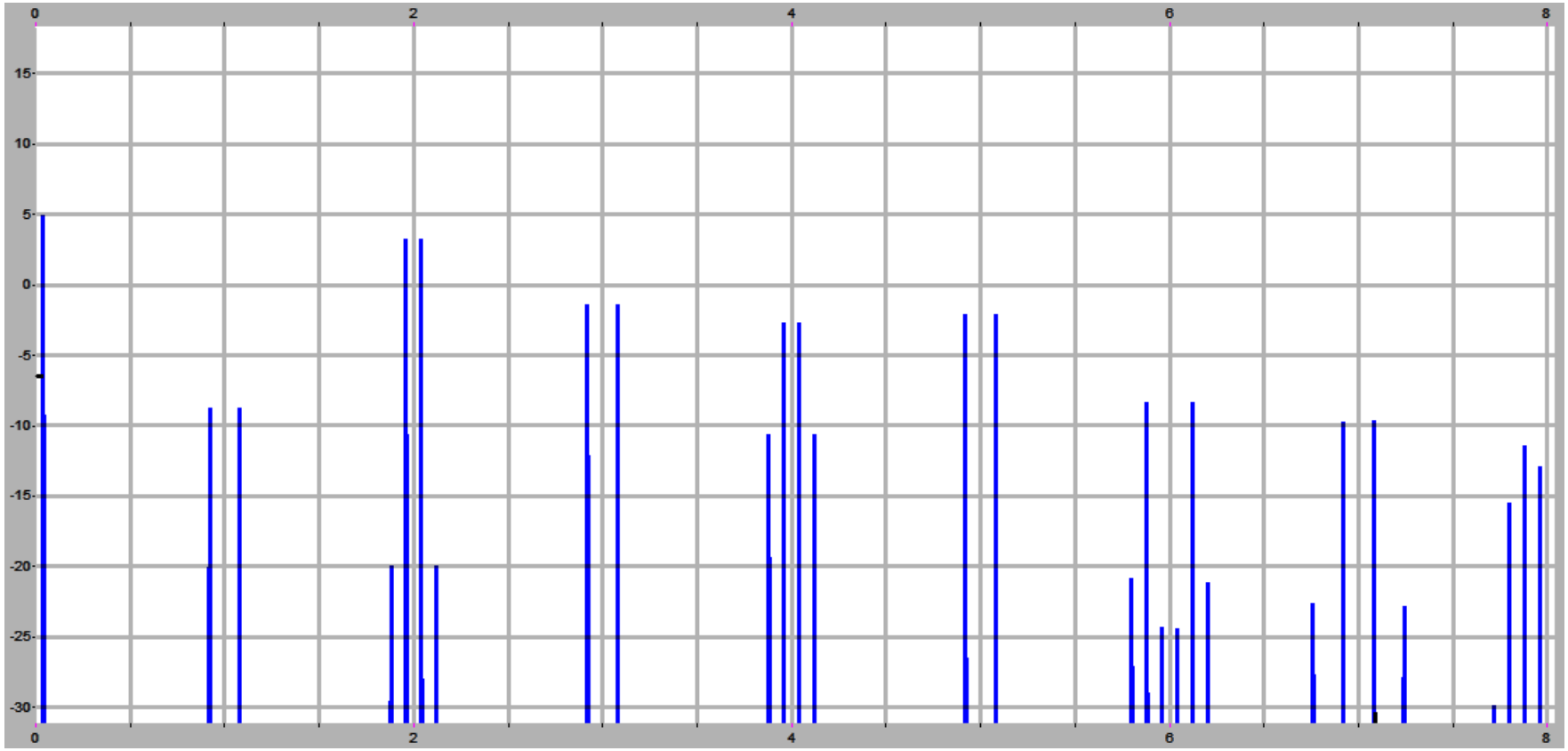
Full-Bridge amplifier in 2 state PWM



Three-state PWM (class BD)



Spectrum of 3-state PWM



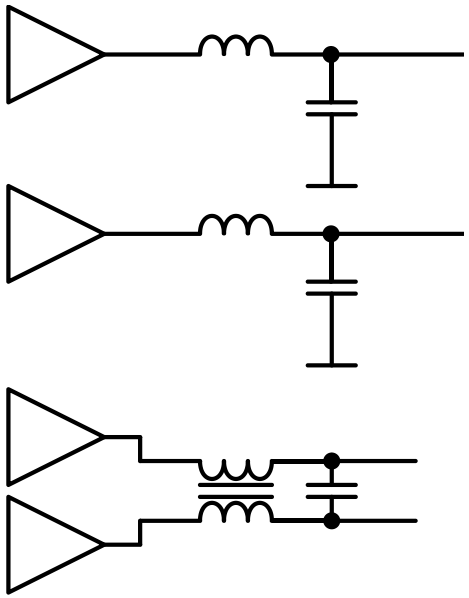
2-State vs 3-State

Three-state...

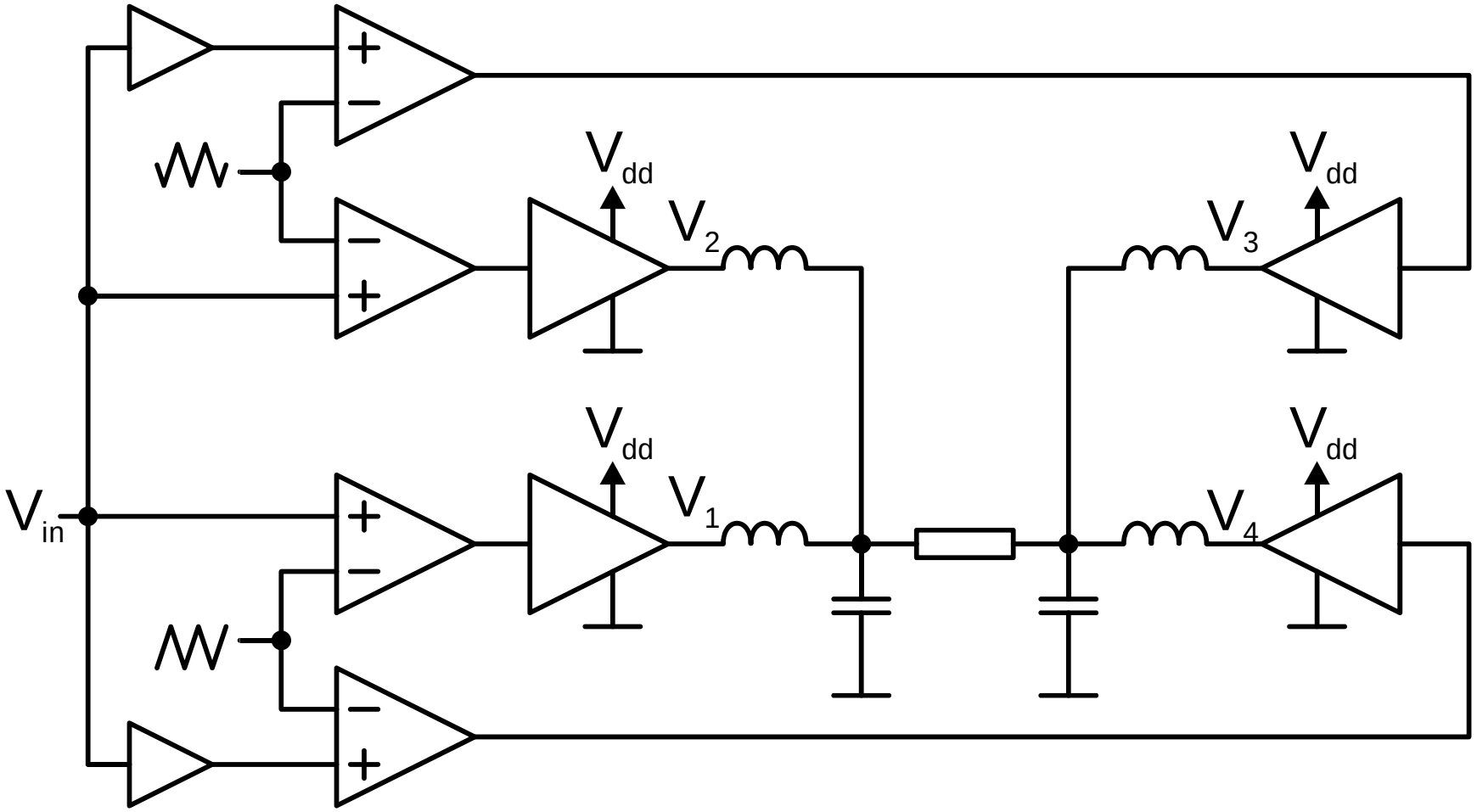
- doubles sampling rate
  - Better efficiency vs bandwidth
- halves open-loop error

Output filter?

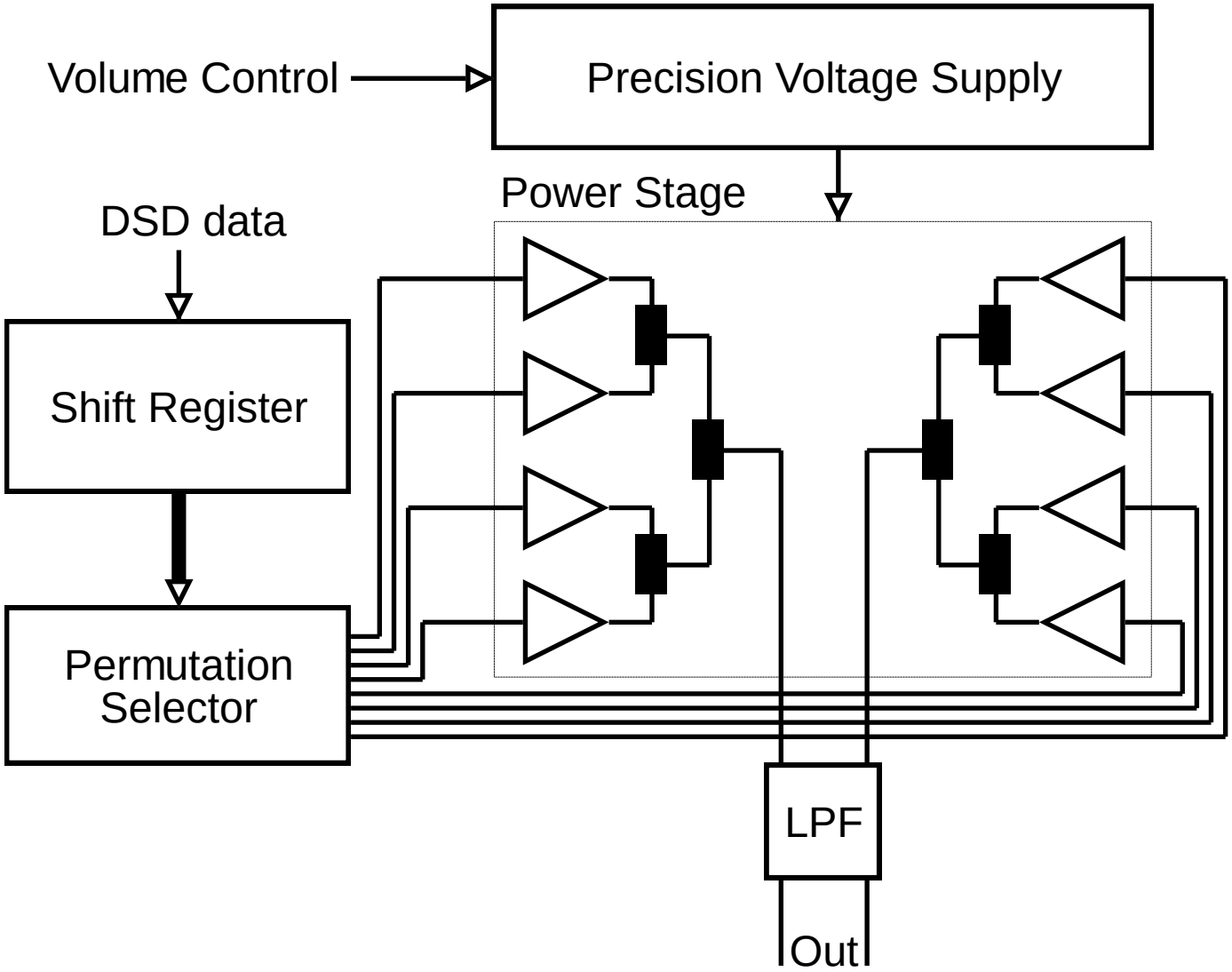
- Single-core
  - no excitation current
  - crossover distortion results
- Two-core
  - excitation current doubles for constant sampling rate



Yet More Phases

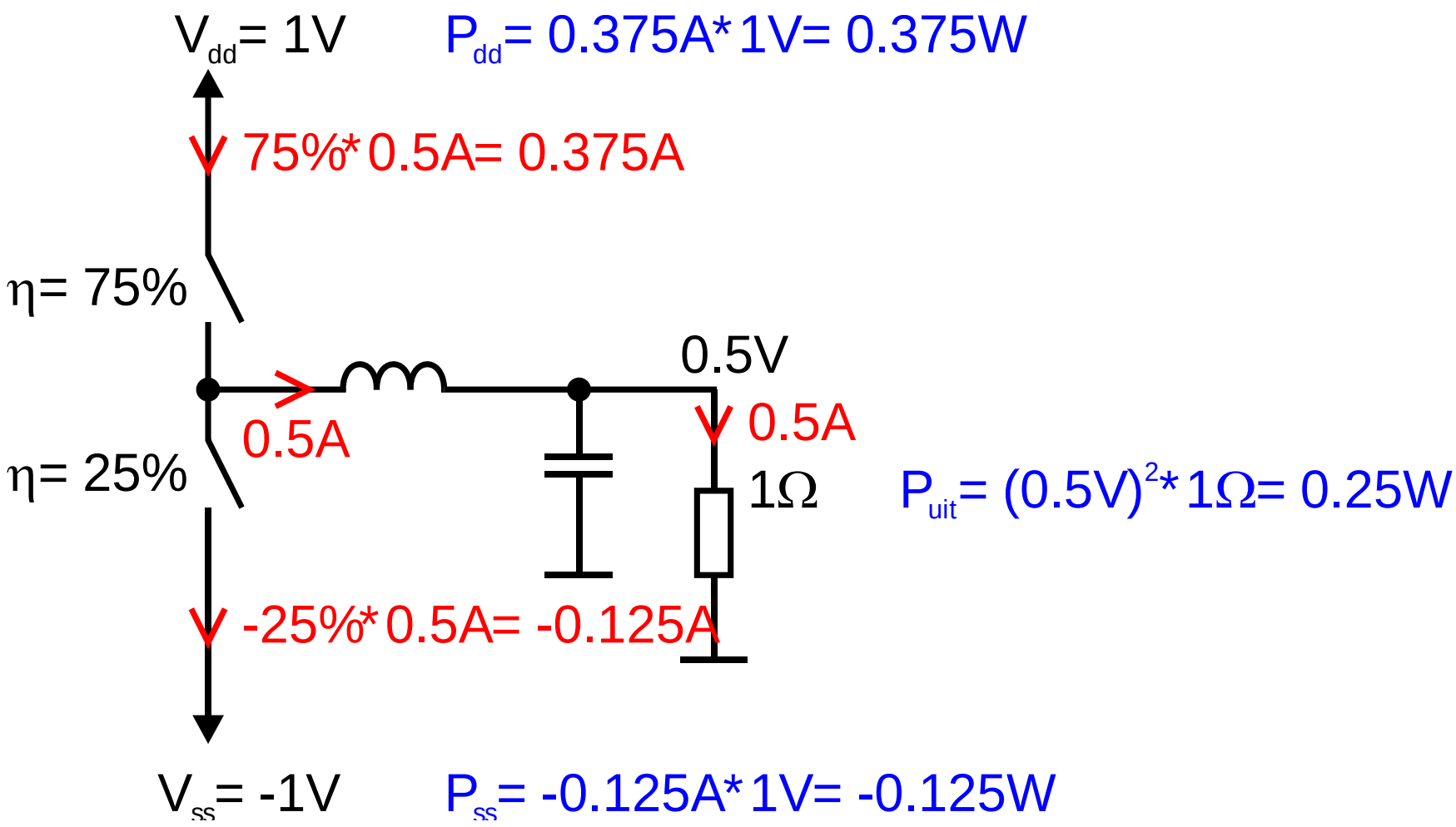


It can get worse...



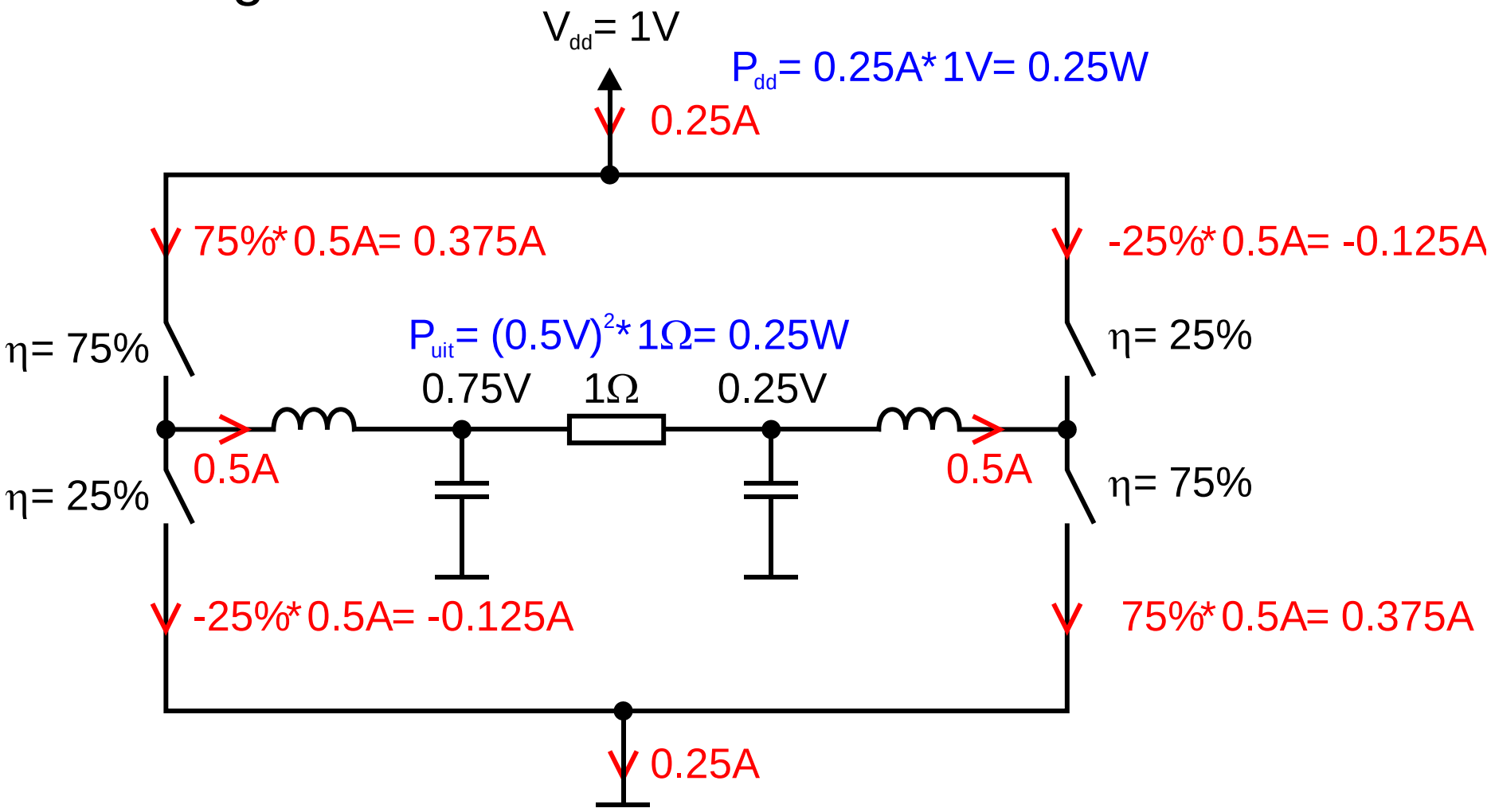
Class D as Power Converter

Half bridge



Class D as Power Converter

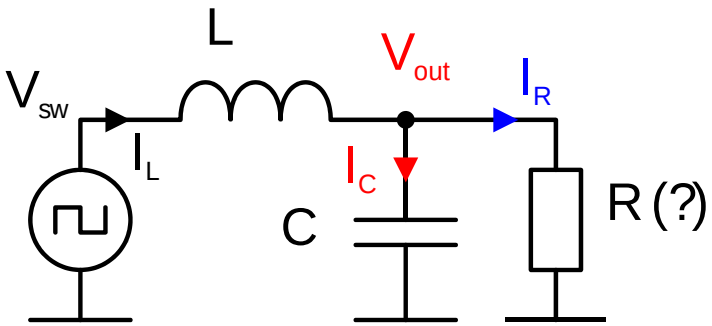
Full bridge

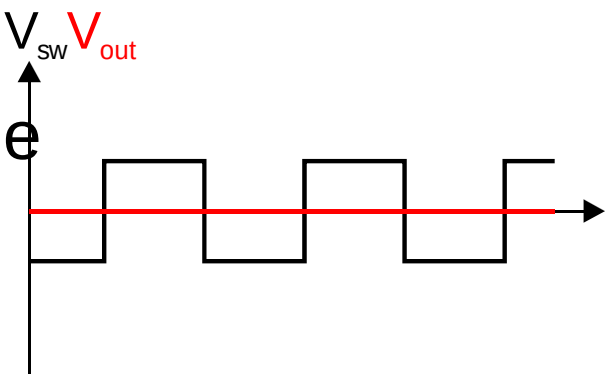


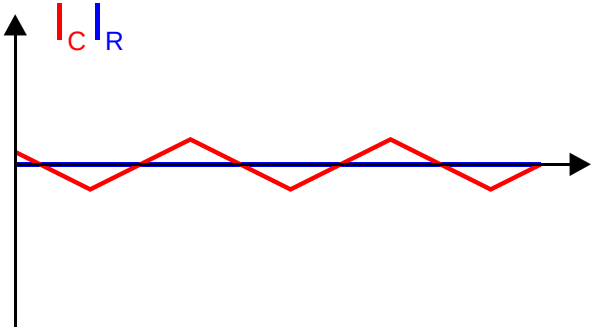
Inductor current

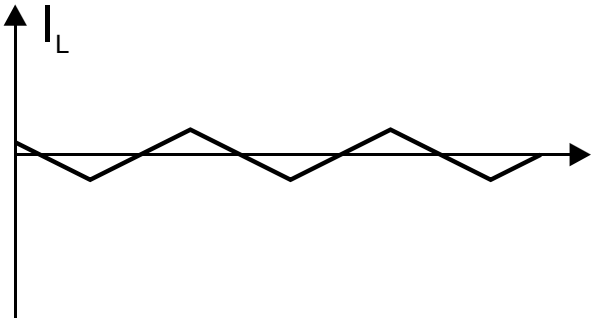
Small modulation index

- Current changes sense every cycle





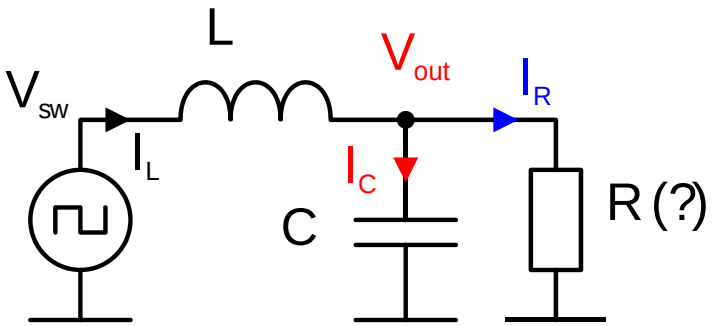


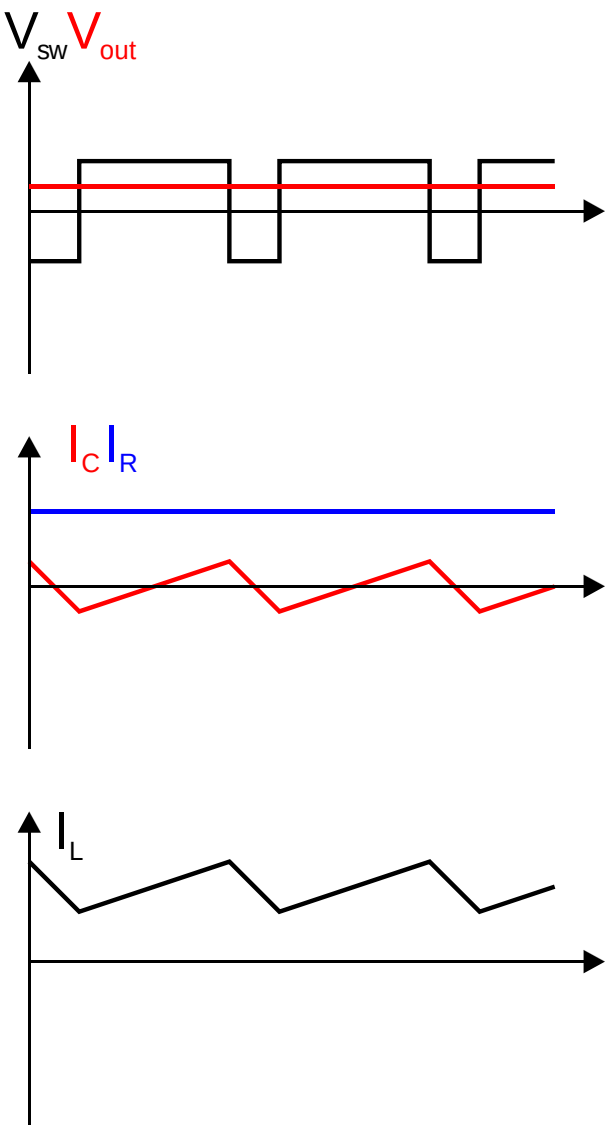


Inductor current

Large modulation index

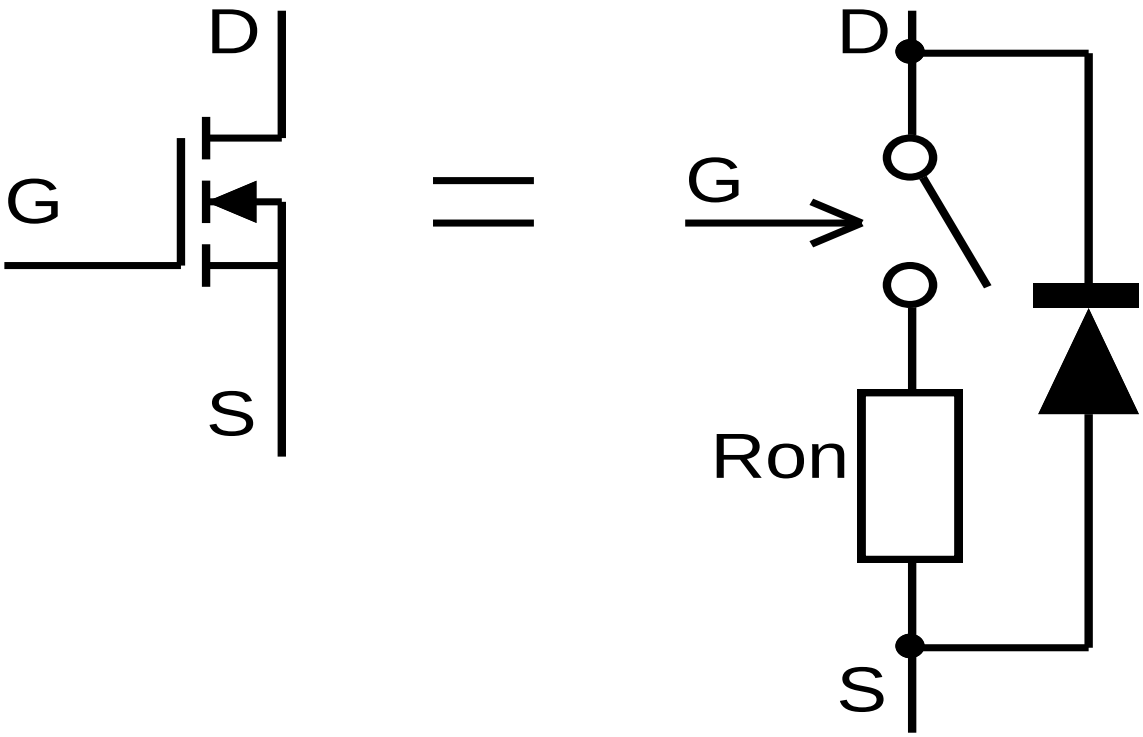
- Current sense does not change





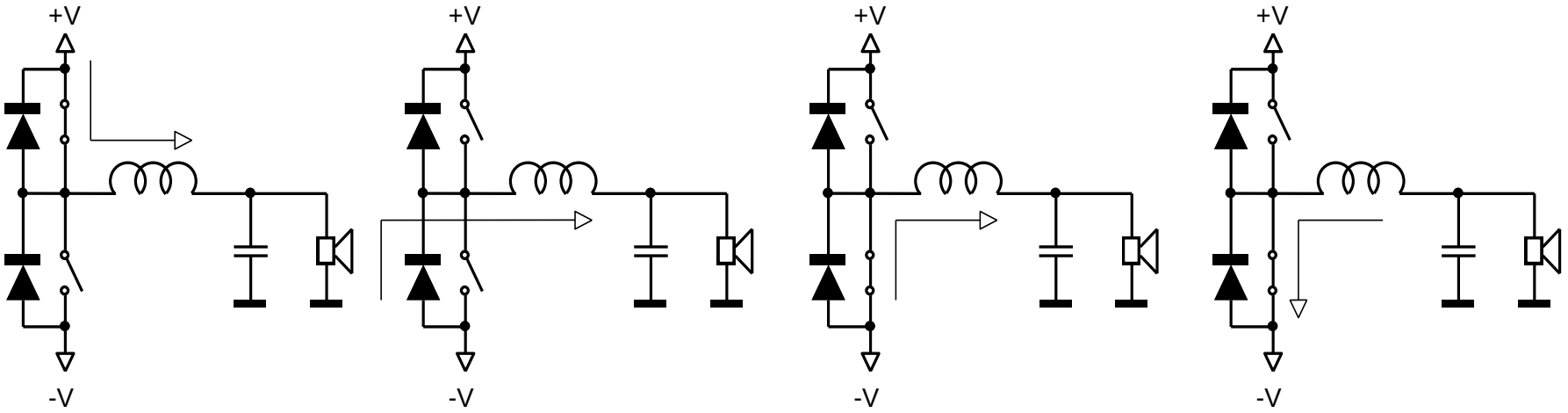
Dead time effects

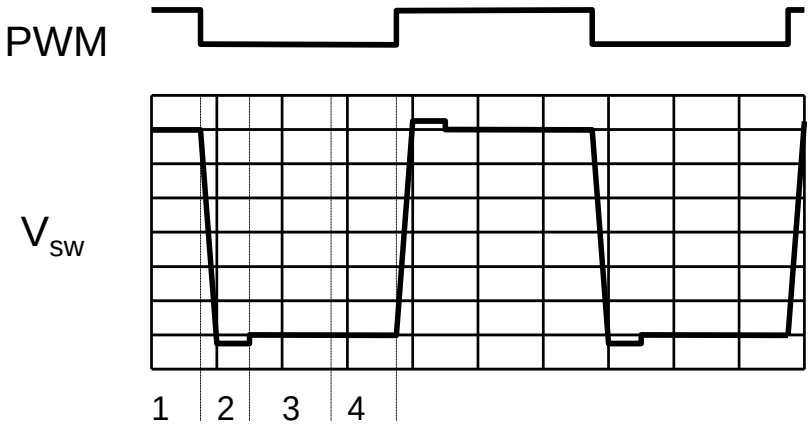
Simplified MOSFET model



Dead time effects

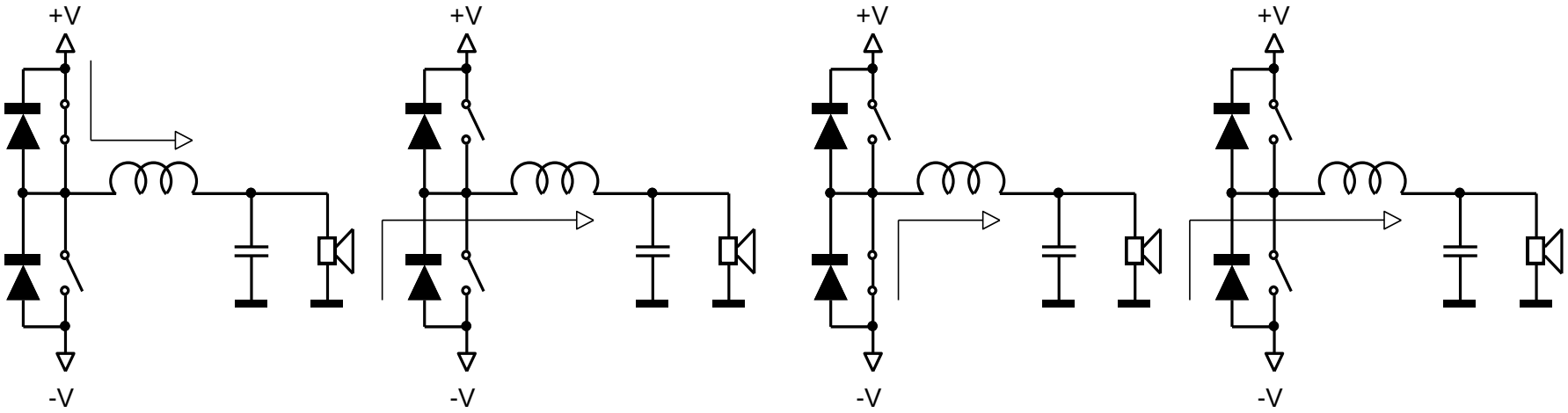
Small modulation index

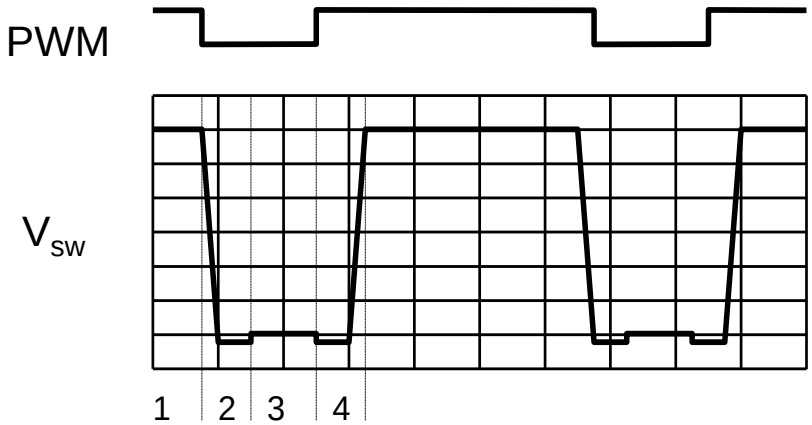




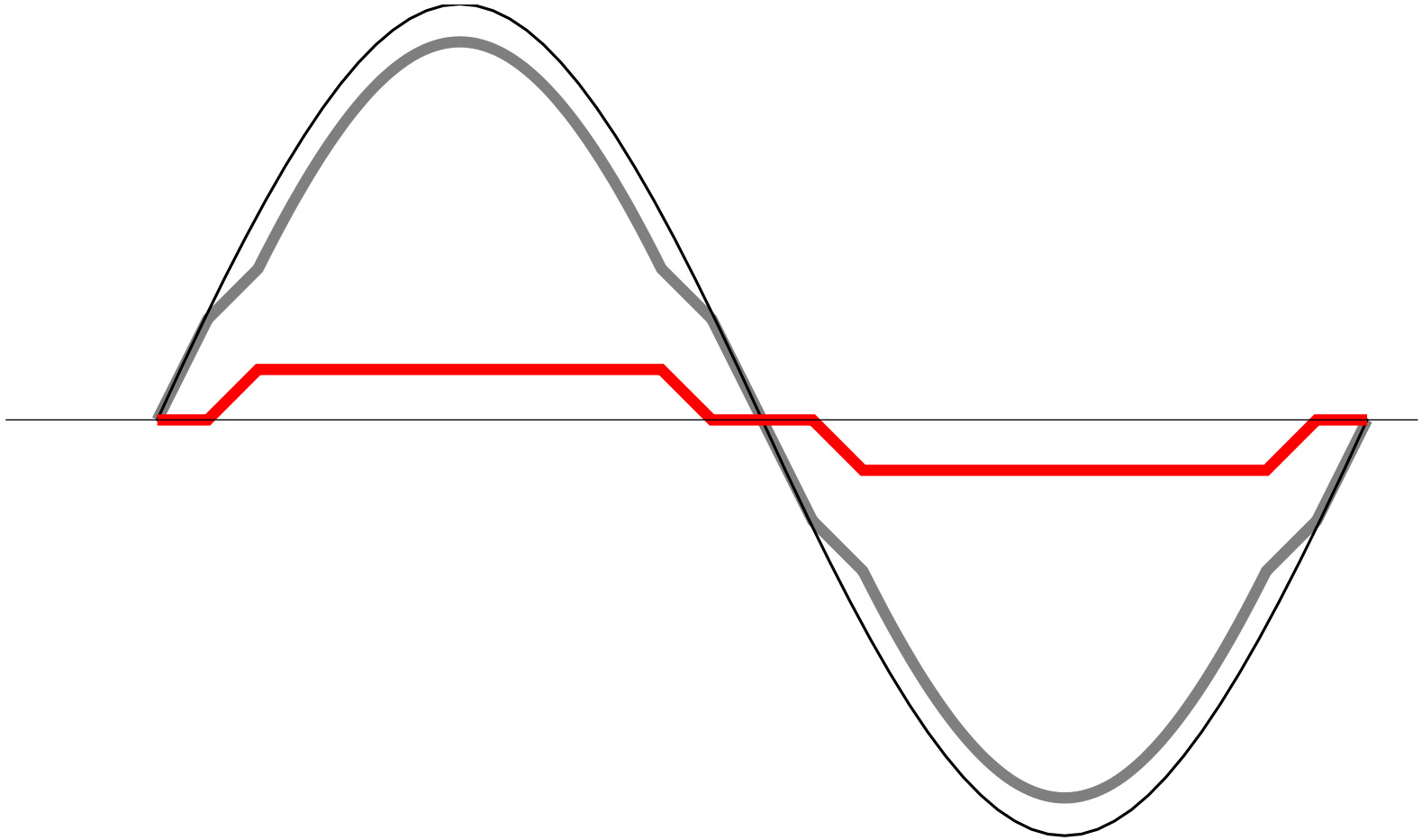
Dead time effects

Large modulation index

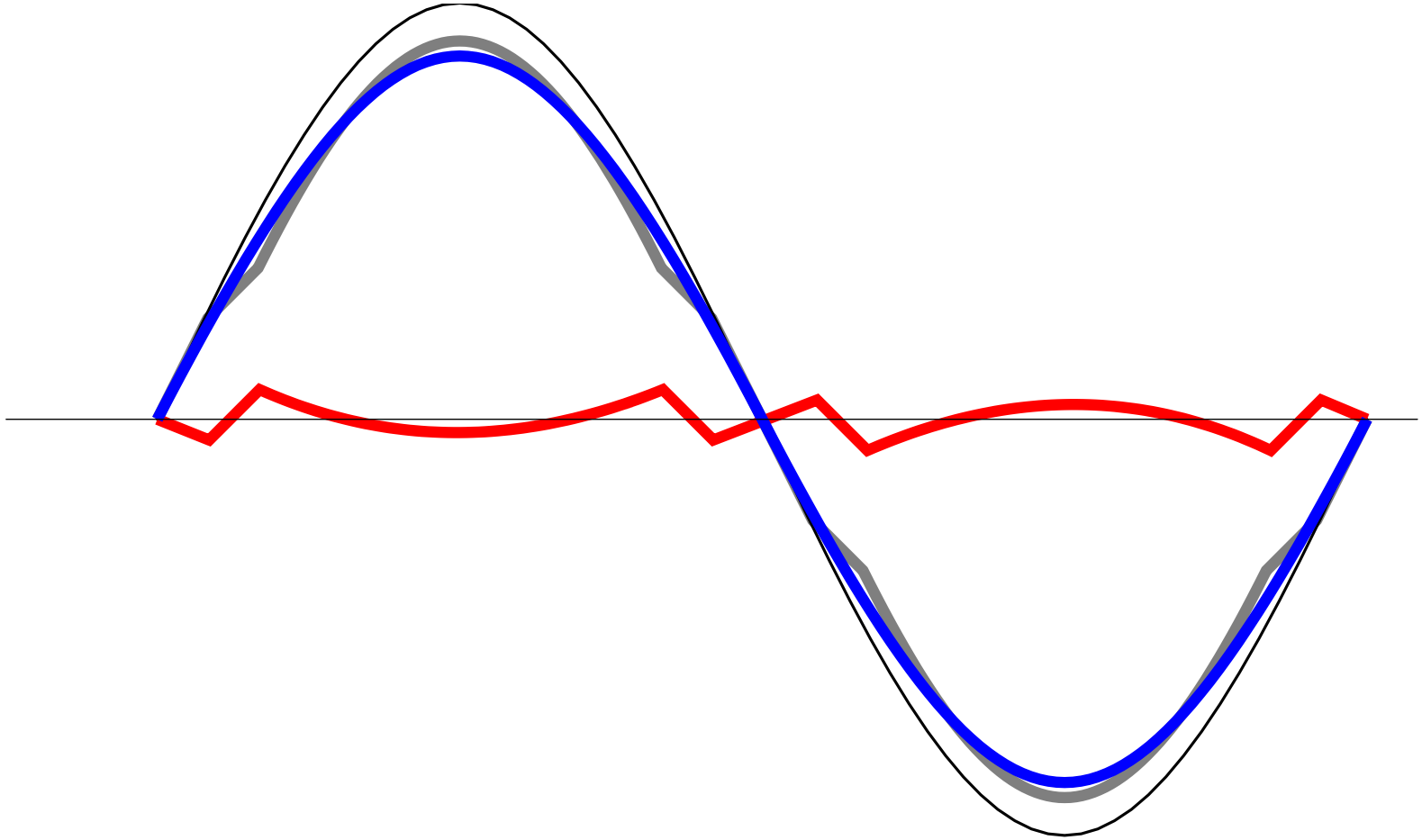




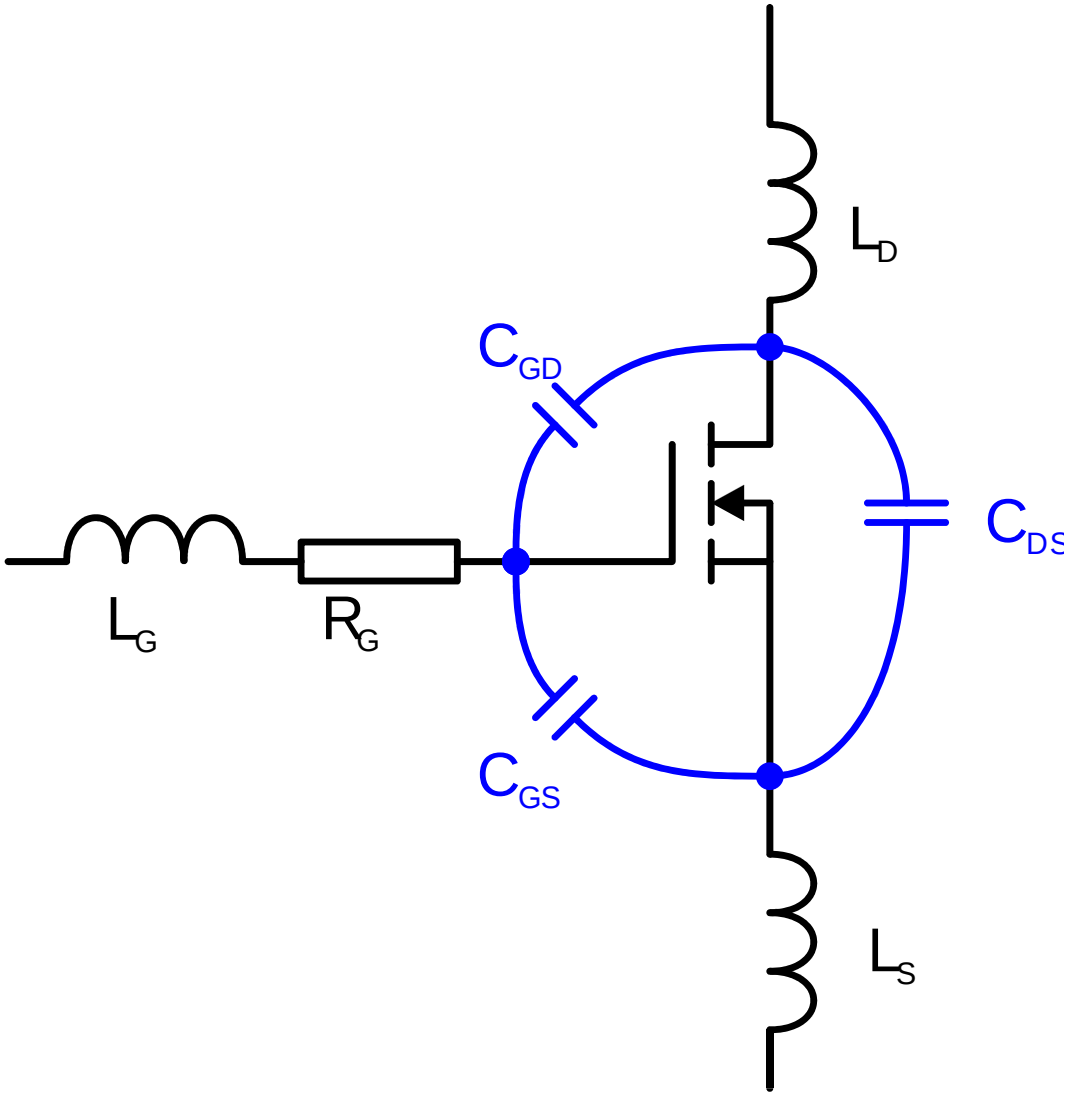
Open-Loop Distortion



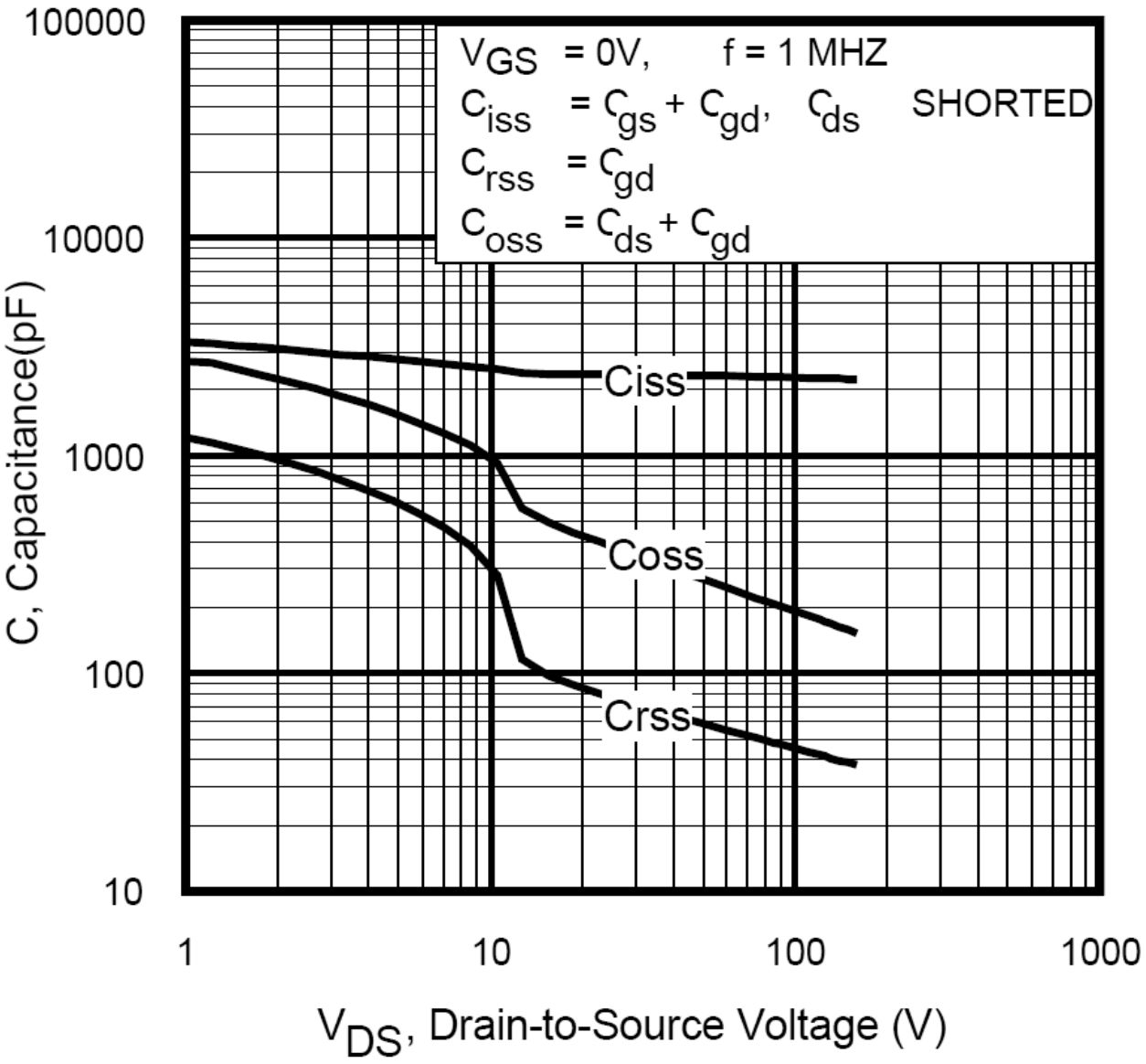
Analyser Reading



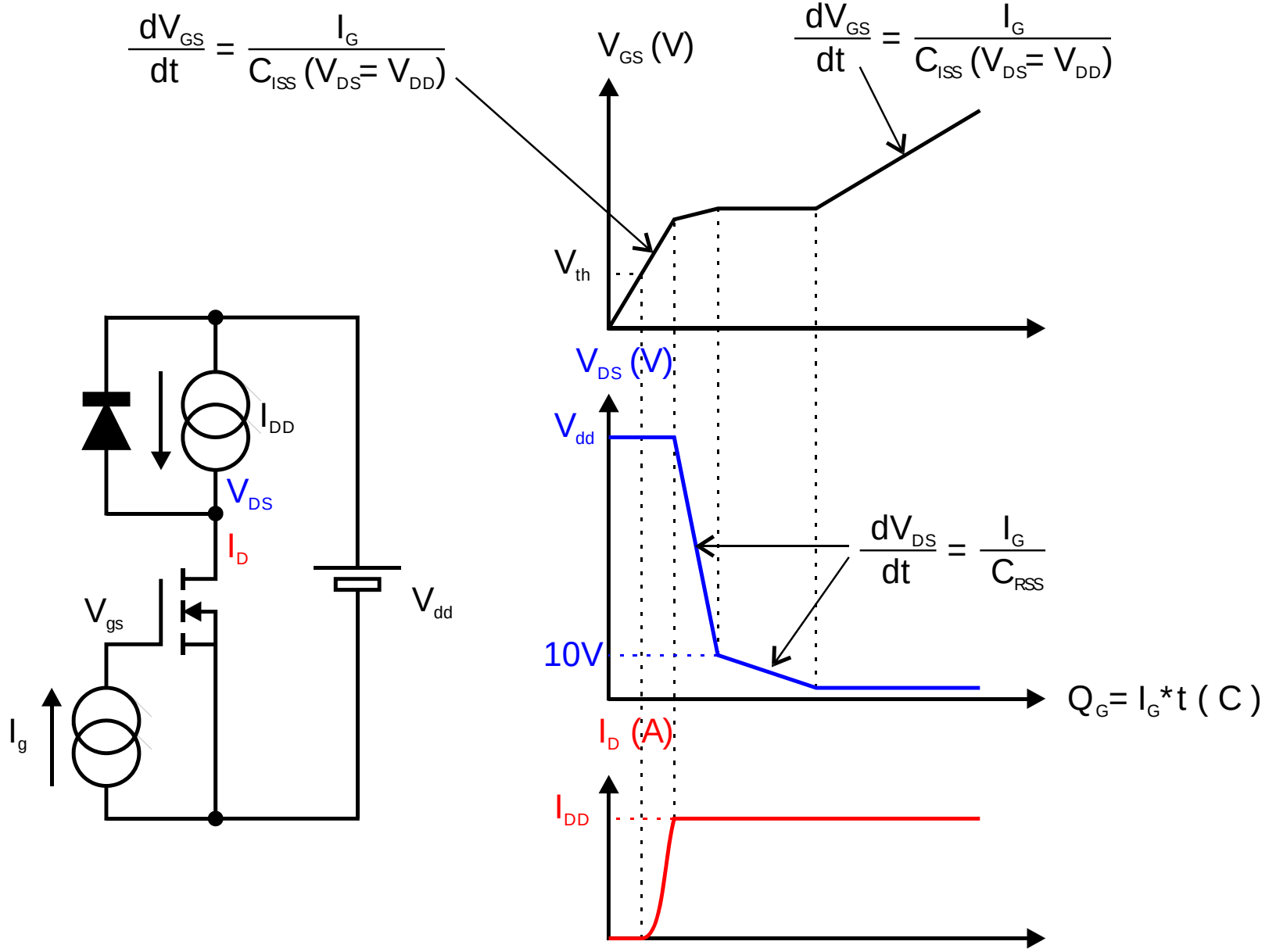
MOSFET parasitics



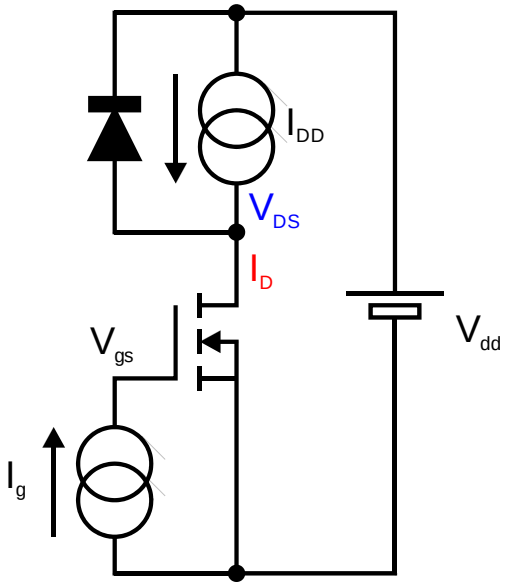
Parasitic capacitances

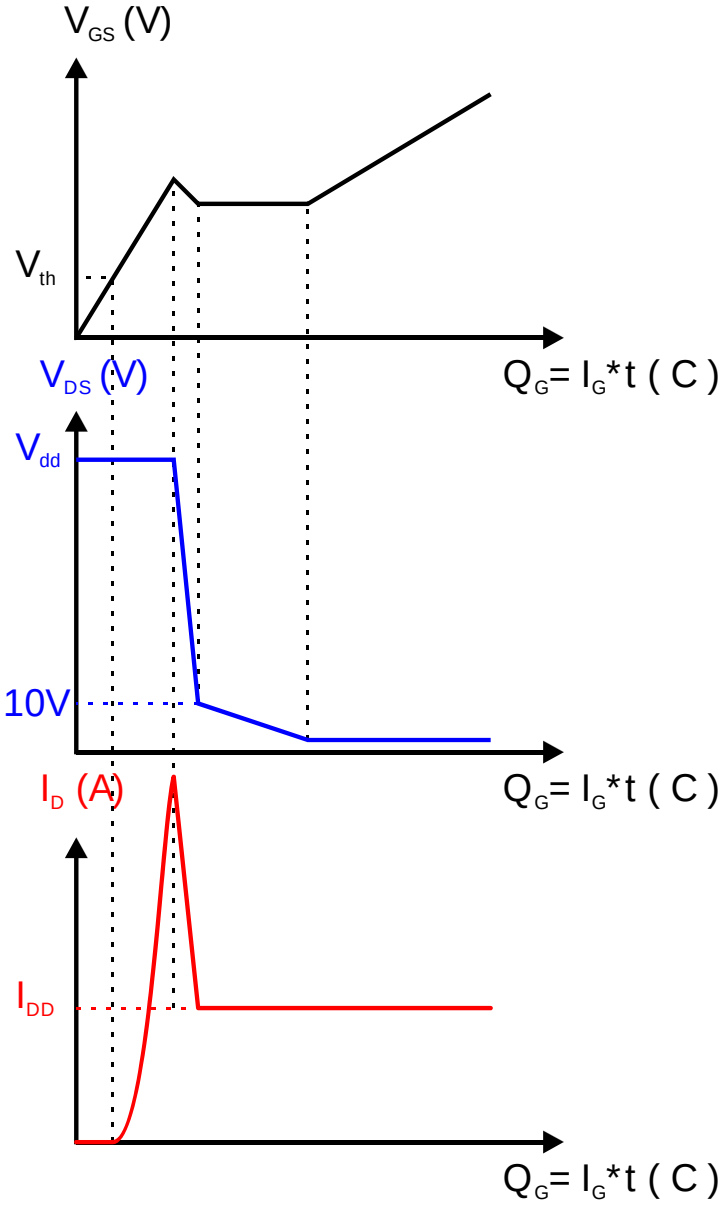


Gate Waveform (hard switching, ideal diode)



Gate Waveform (real diode)





Gate Gotchas

Until and during recovery

- Dissipated power = Vcc*Qrr
- Vds=Vcc
- Gate capacitance is low
- But we’d like to go slow

After recovery

- Vds<Vgs
- Gate capacitance is high
- Dissipated power = Vds*Id*time
- We’d like to finish quickly

Current limiting gate driver works the wrong way round.

Output filter

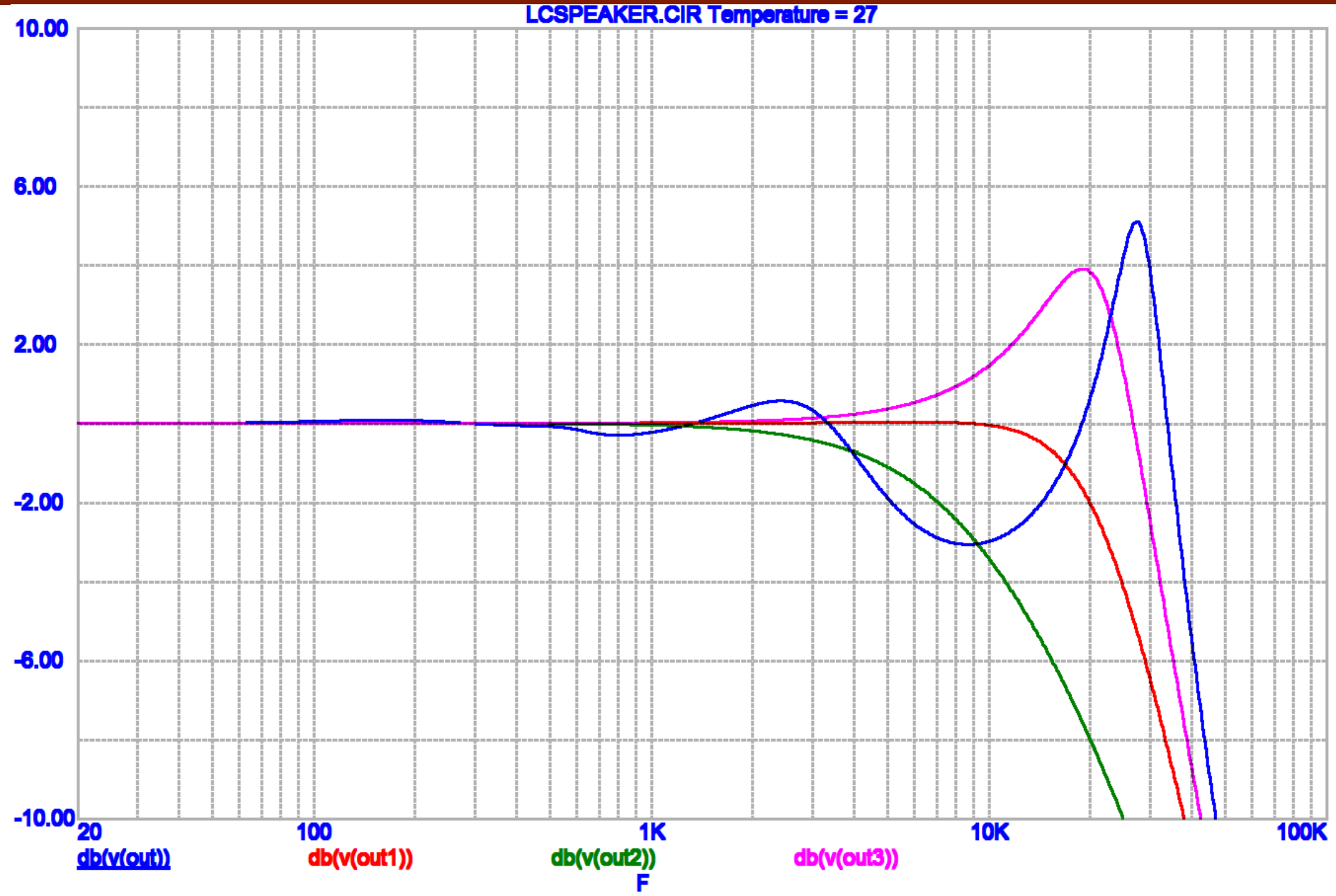
Desired function

- Attenuate the carrier

Undesired functions

- Restrict bandwidth
- Increase output impedance
- Modify the frequency response
- Add distortion

Load response of 2nd order LPF



Output Filter

The optimisation problem

- Reduce Z_{out} ➔ Increase f_c ➔ Reduce attenuation
- Improve Bandwidth ➔ Increase f_c ➔ Reduce attenuation
- Improve Flatness ➔ Increase f_c ➔ Reduce attenuation
- Reduce distortion ➔ Reduce L ➔ Reduce attenuation

The root cause

- Controlled variable is an internal node
- Output voltage is uncontrolled

Summary of (analogue!) nonidealities

Power Supply Rejection

- PWM power stage is an AM modulator

Switch Timing

- Dead time causes distortion

Output Filter

- Output impedance is infinity at fc
- Inductor is non-linear

Feedback

Solves many problems at once

- Output impedance (post LPF only)
- Distortion
- Frequency response (post LPF only)

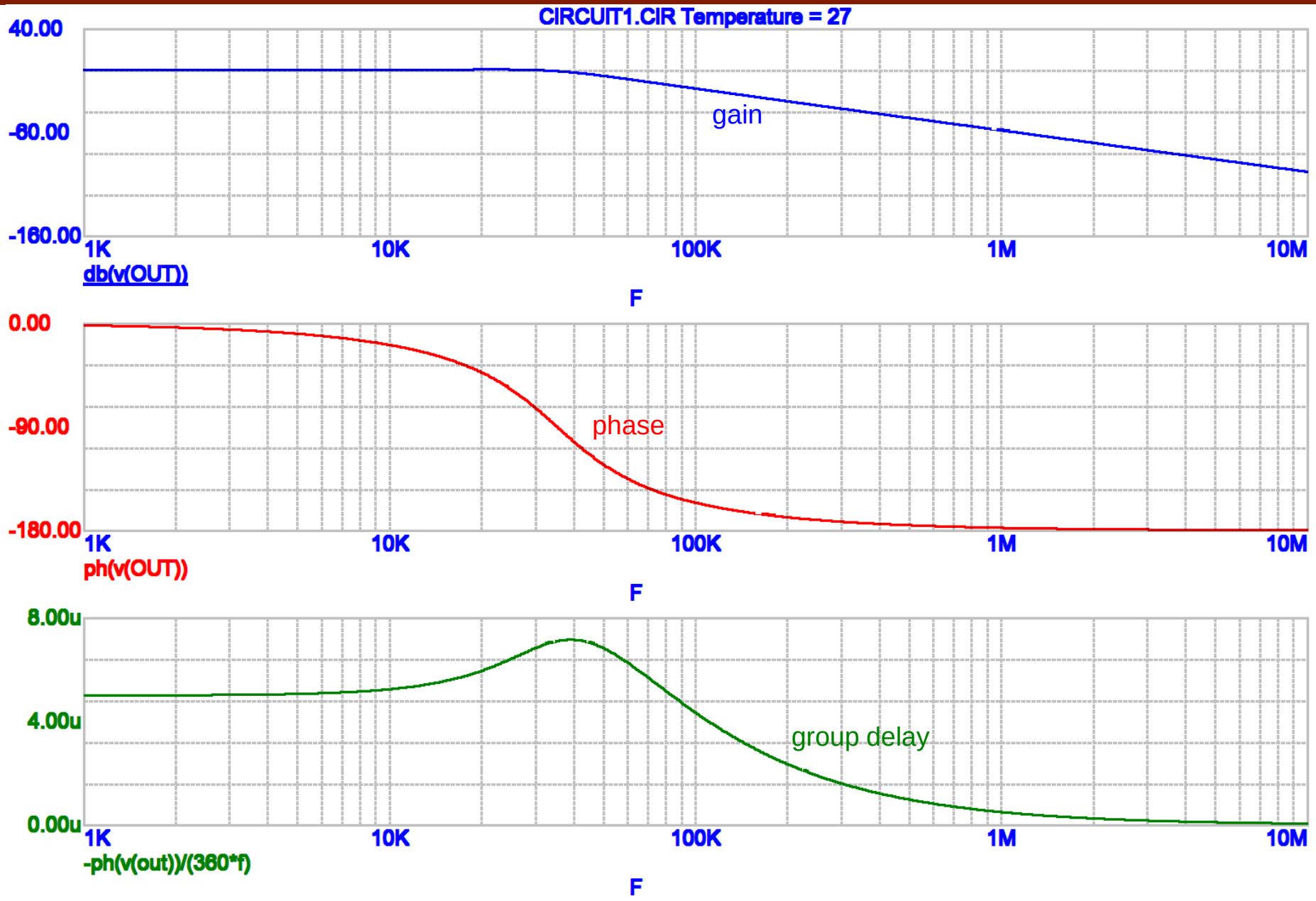
Why many don’t use it

- Audio folk lore
  - “Feedback sounds bad”
  - “Class D is Digital”

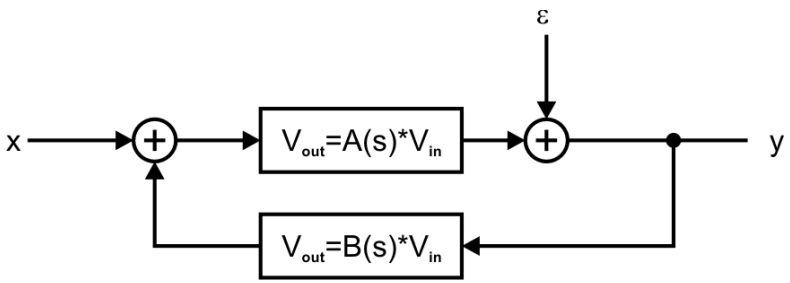
Why global feedback is even rarer

- LC phase shift considered “insurmountable”
- No “rules of thumb”

Delay in the LC filter?



Some control theory basics



$$y = \varepsilon + A(s)\cdot\left(x + B(s)\cdot y\right)$$

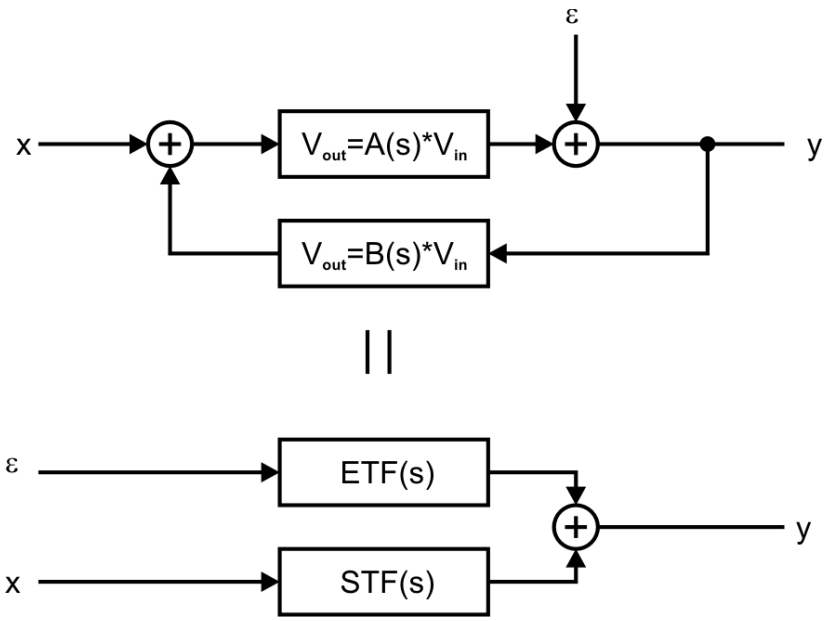
$$\Updownarrow$$

$$y - A(s)\cdot B(s)\cdot y = \varepsilon + A(s)\cdot x$$

$$\Updownarrow$$

$$y = \frac{\varepsilon + A(s)\cdot x}{1 - A(s)\cdot B(s)} = \frac{\varepsilon}{1 - A(s)\cdot B(s)} + \frac{A(s)\cdot x}{1 - A(s)\cdot B(s)}$$

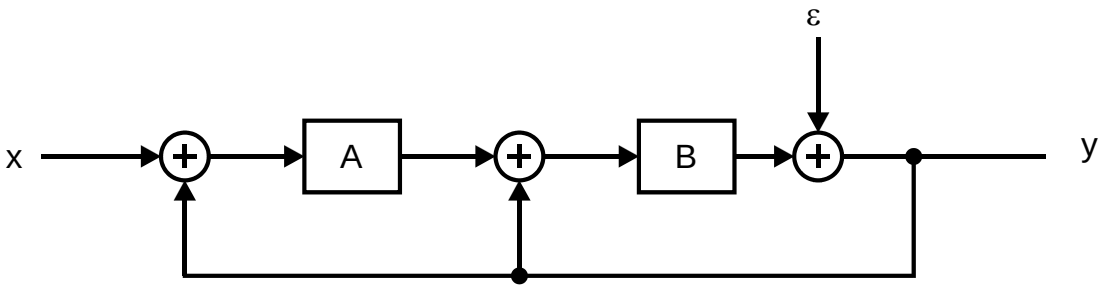
ETF & STF



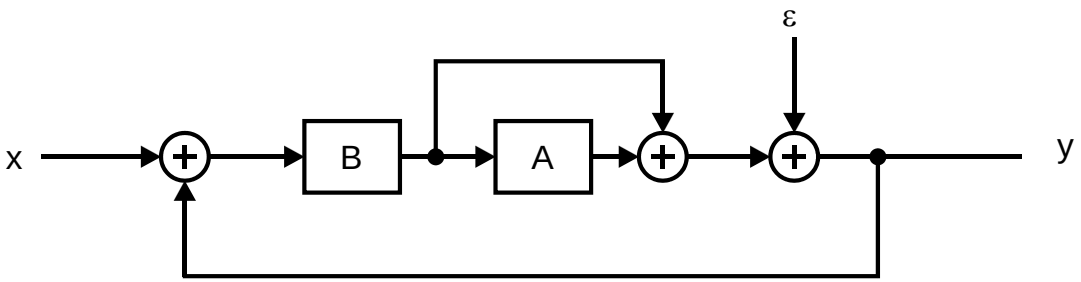
$$ETF(s) = \frac{1}{1 - A(s) \cdot B(s)}$$

$$STF(s) = \frac{A(s)}{1 - A(s) \cdot B(s)}$$

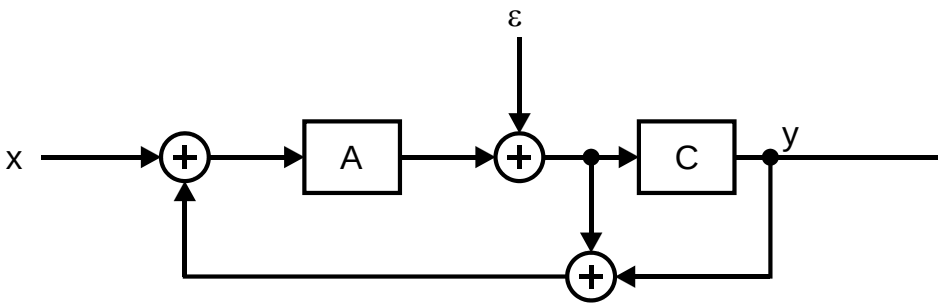
Various permutations



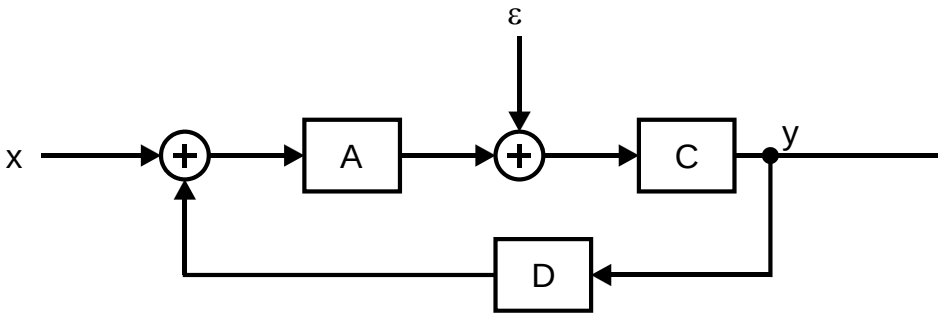
$$y = \frac{A \cdot B}{1 - B - A \cdot B} \cdot x + \frac{1}{1 - B - A \cdot B} \cdot \varepsilon$$



$$y = \frac{B + A \cdot B}{1 - B - A \cdot B} \cdot x + \frac{1}{1 - B - A \cdot B} \cdot \varepsilon$$

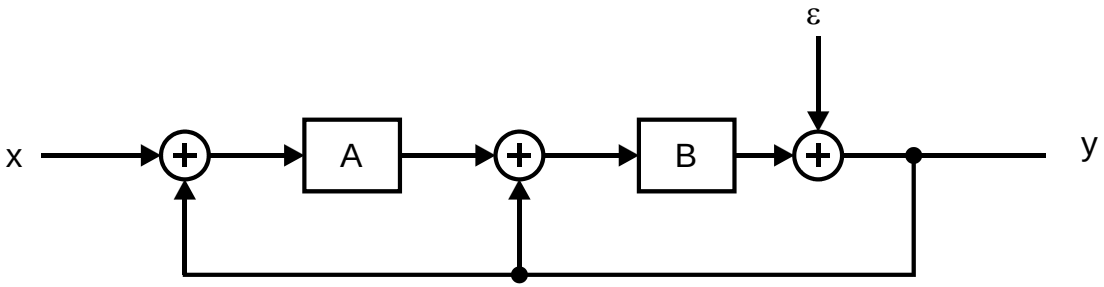


$$y = \frac{A \cdot C}{1 - A - A \cdot C} \cdot x + C \cdot \frac{1}{1 - A - A \cdot C} \cdot \varepsilon$$



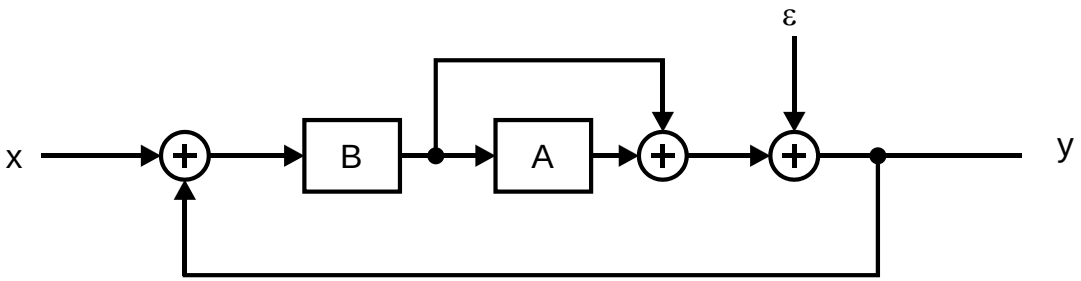
$$y = \frac{A \cdot C}{1 - A \cdot C \cdot D} \cdot x + C \cdot \frac{1}{1 - A \cdot C \cdot D} \cdot \varepsilon$$

Various permutations



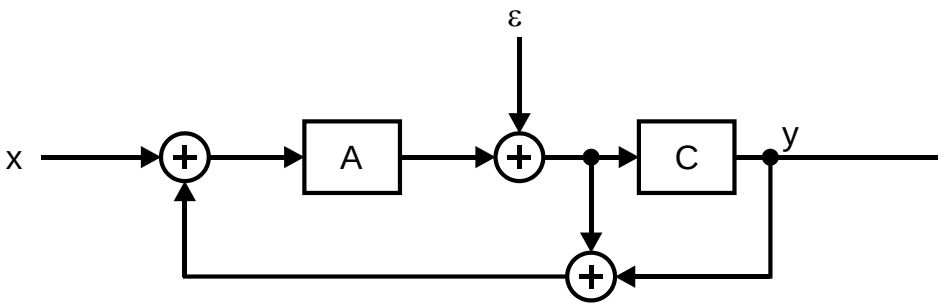
$$A_L = B + A \cdot B$$

$$y = \frac{A \cdot B}{1 - A_L} \cdot x + \frac{1}{1 - A_L} \cdot \varepsilon$$



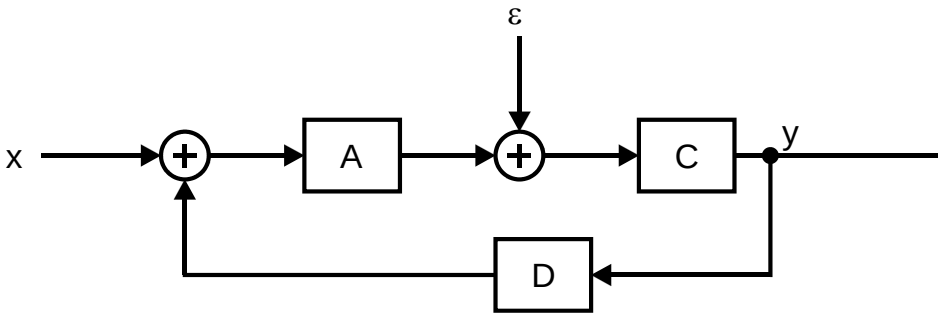
$$A_L = B + A \cdot B$$

$$y = \frac{A_L}{1 - A_L} \cdot x + \frac{1}{1 - A_L} \cdot \varepsilon$$



$$A_L = A + A \cdot C$$

$$y = \frac{A \cdot C}{1 - A_L} \cdot x + C \cdot \frac{1}{1 - A_L} \cdot \varepsilon$$



$$A_L = A \cdot C \cdot D$$

$$y = \frac{A \cdot C}{1 - A_L} \cdot x + C \cdot \frac{1}{1 - A_L} \cdot \varepsilon$$

Loop needs

ETF must be stable and not have excessive gain

- Poles well left of imaginary axis

ETF must have very low gain in audio band

- Zeros close to or on imaginary axis

Loop function A_L

- Loop poles=zeros of ETF
- Loop zeros must be freely settable

Universal loop control function

If A_L ...

- has n poles and n-1 zeros
- has independantly settable zeros

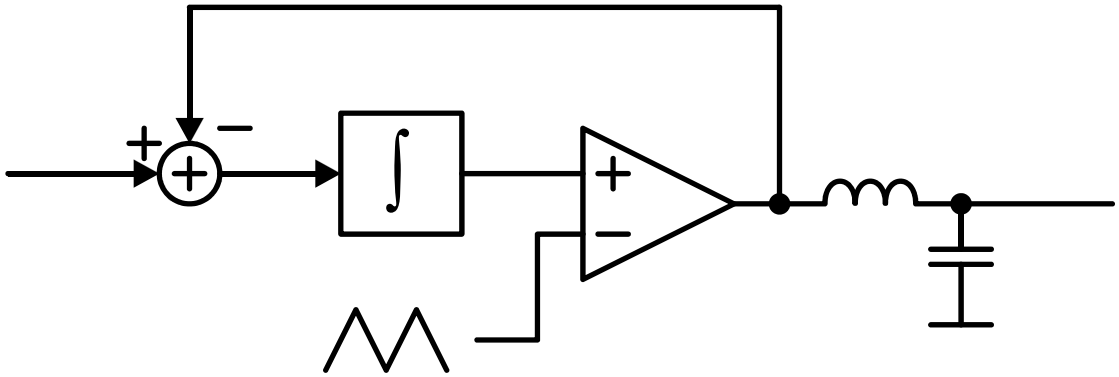
...then

- a stable loop is always possible

$$A_L(s) = k \cdot \frac{\prod_{i=1}^{n-1}(s - z_i)}{\prod_{i=1}^{n}(s - p_i)} = \frac{\sum_{i=0}^{n-1} a_i \cdot s^i}{\sum_{i=0}^{n} b_i \cdot s^i}$$

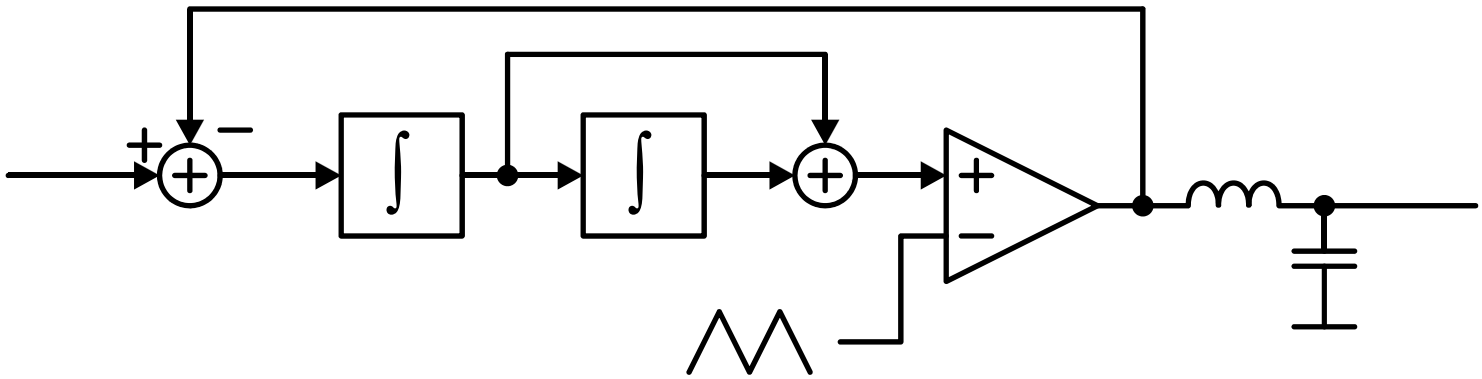
Typical loops

1 pole, no zeros, pre-filter f/b only



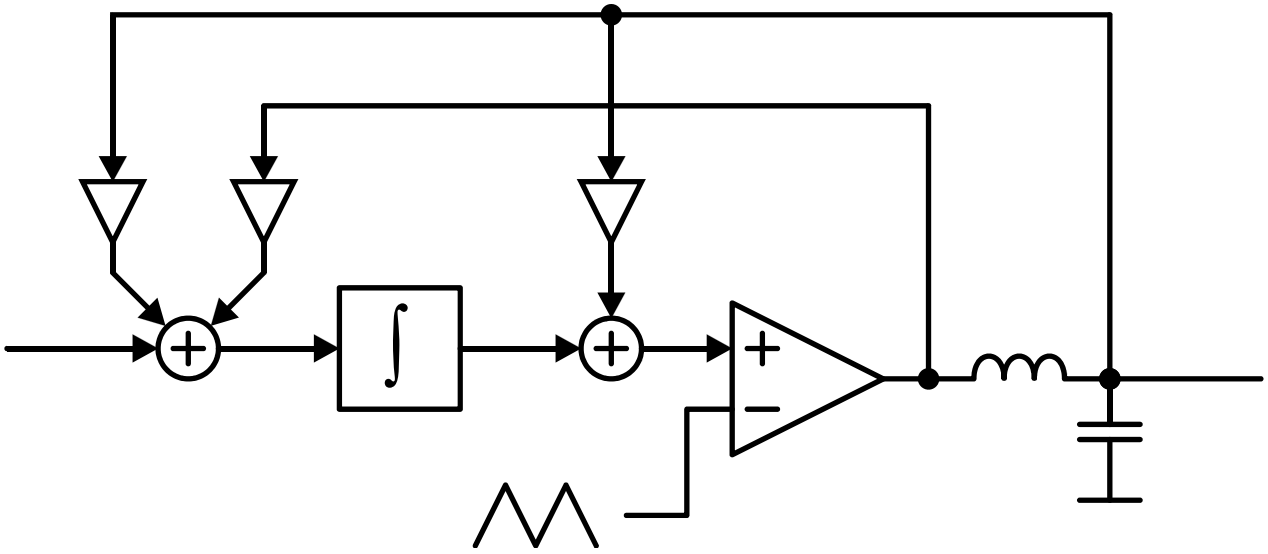
Typical loops

2 poles, 1 zero, pre-filter f/b only



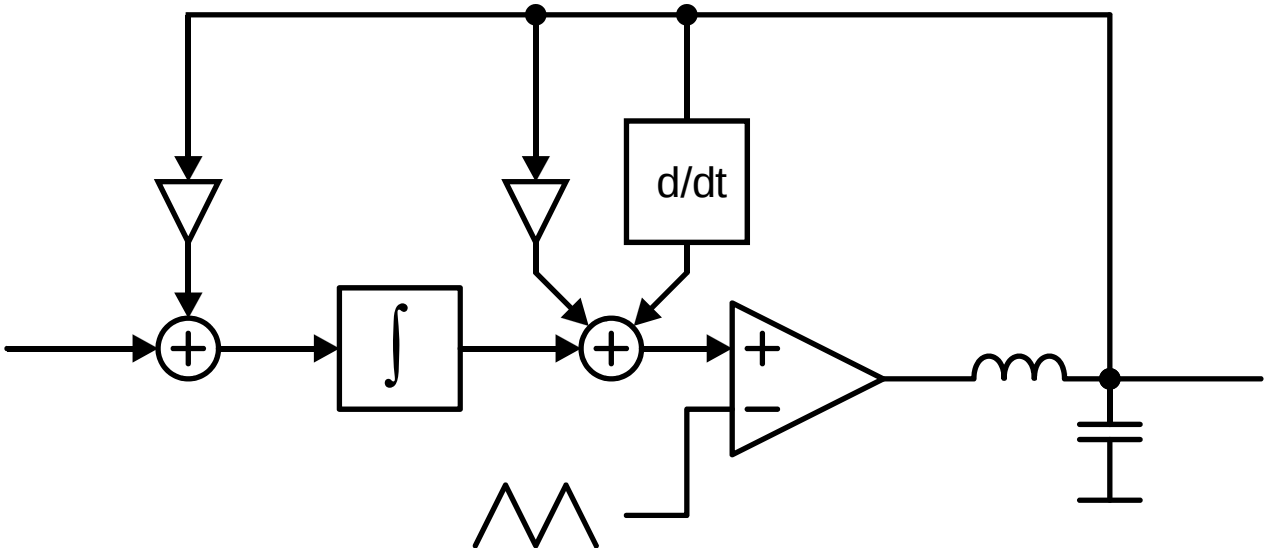
Typical loops

3 poles, 2 zeros, mixed feedback



Typical loops

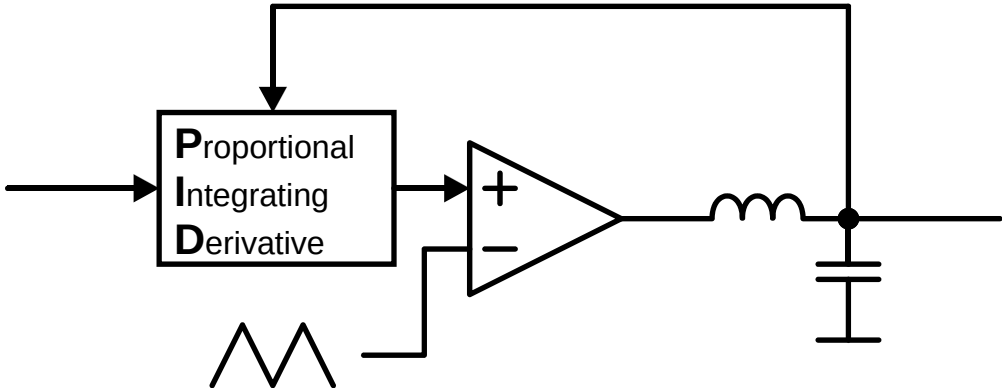
3 poles, 2 zeros, global feedback



...also known as...:

Typical loops

...PID!



PI(I...)D control for global loops

Pro

- Very low output impedance
- Minimum 3rd order loop
  - Large loop gain
- Nonlinear distortion from inductor is reduced
- Known art

Contra

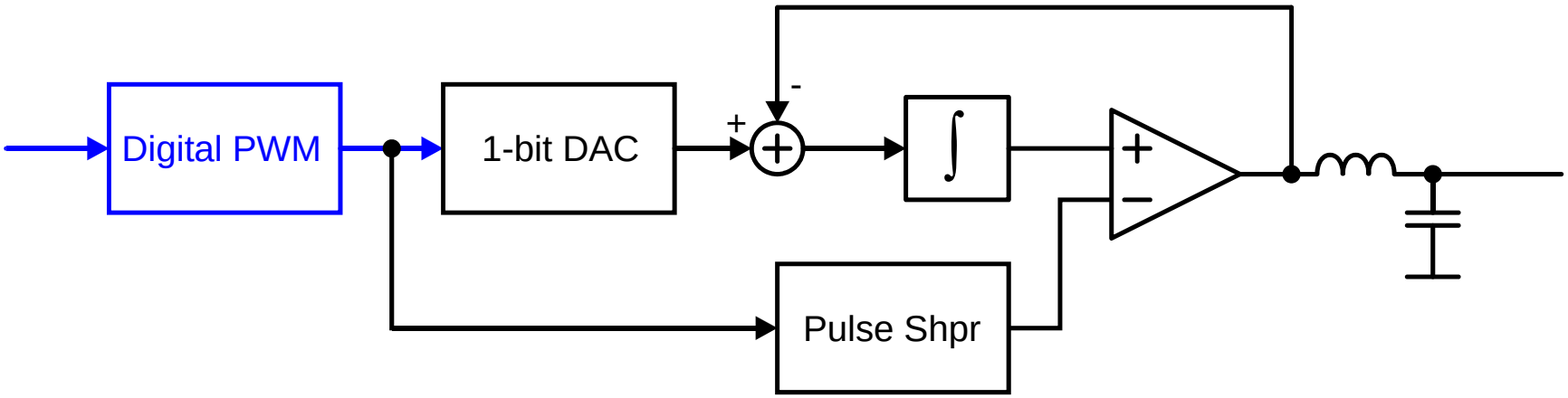
- Can’t get away with bad PCB layout

No good excuses for not using global feedback

Pre-LC and mixed f/b are provably suboptimal

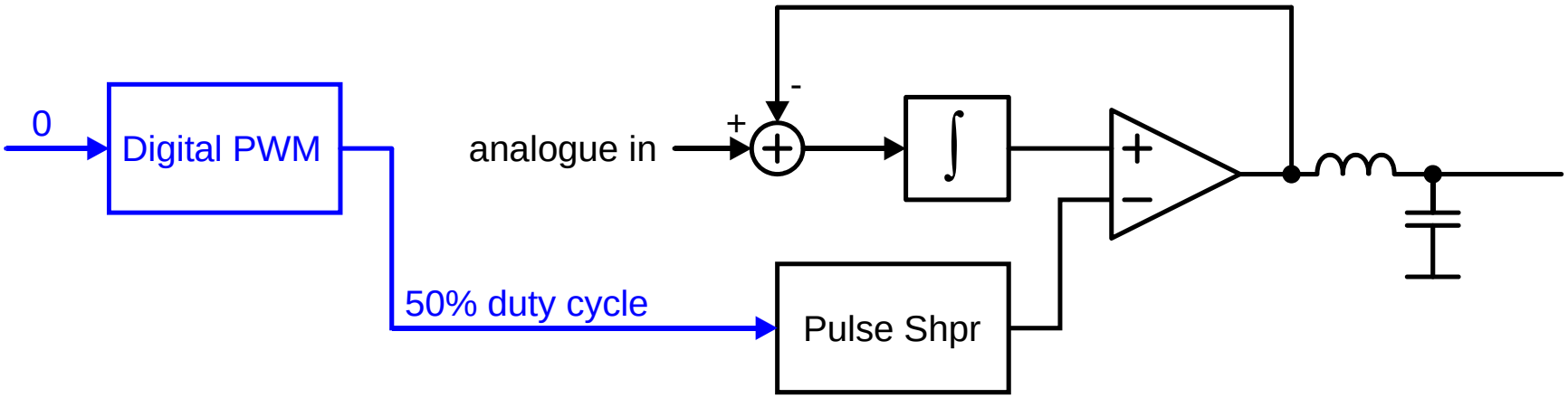
Rearranged loops

Digital PWM + local loop (“edge error correction”)



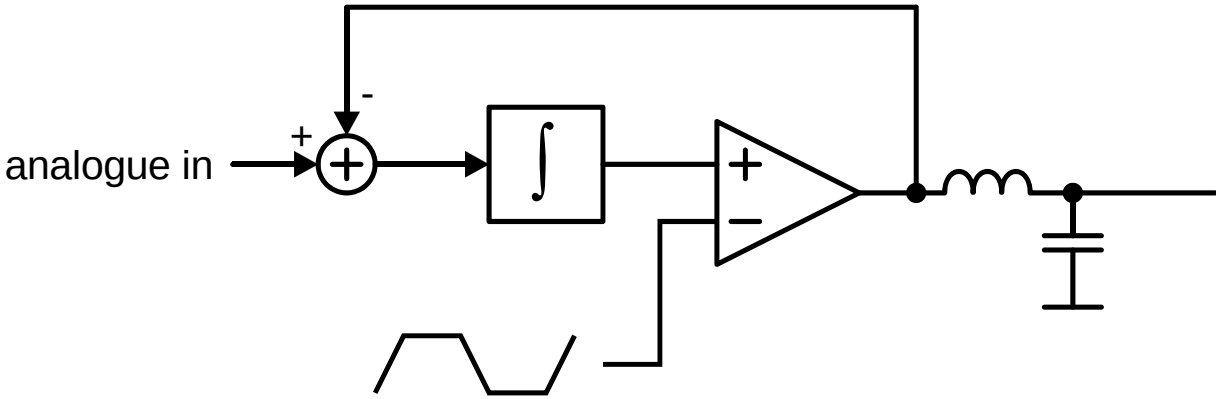
Rearranged loops

Hidden “analogue” amplifier:



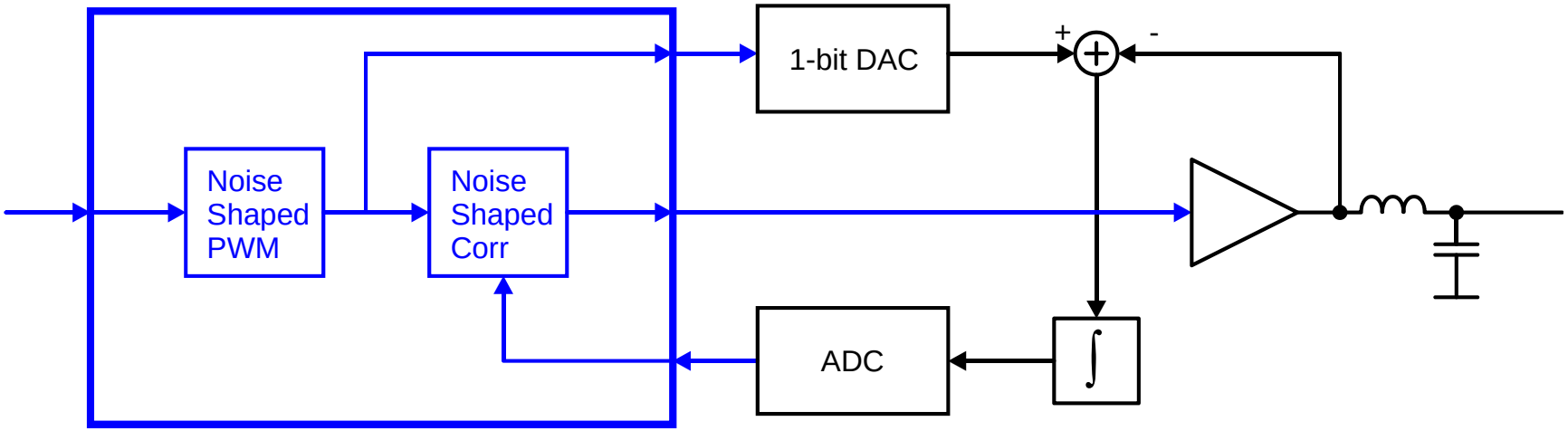
Rearranged loops

No news at all, really:



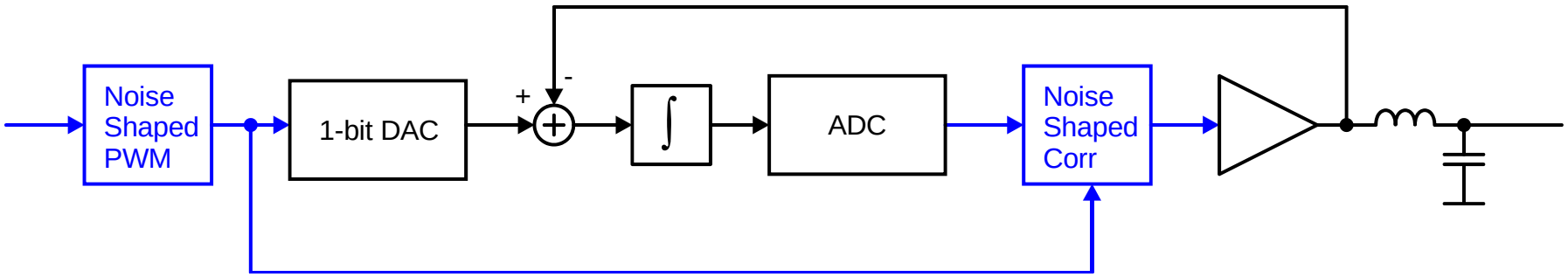
Rearranged loops

Indirect “digital feedback”

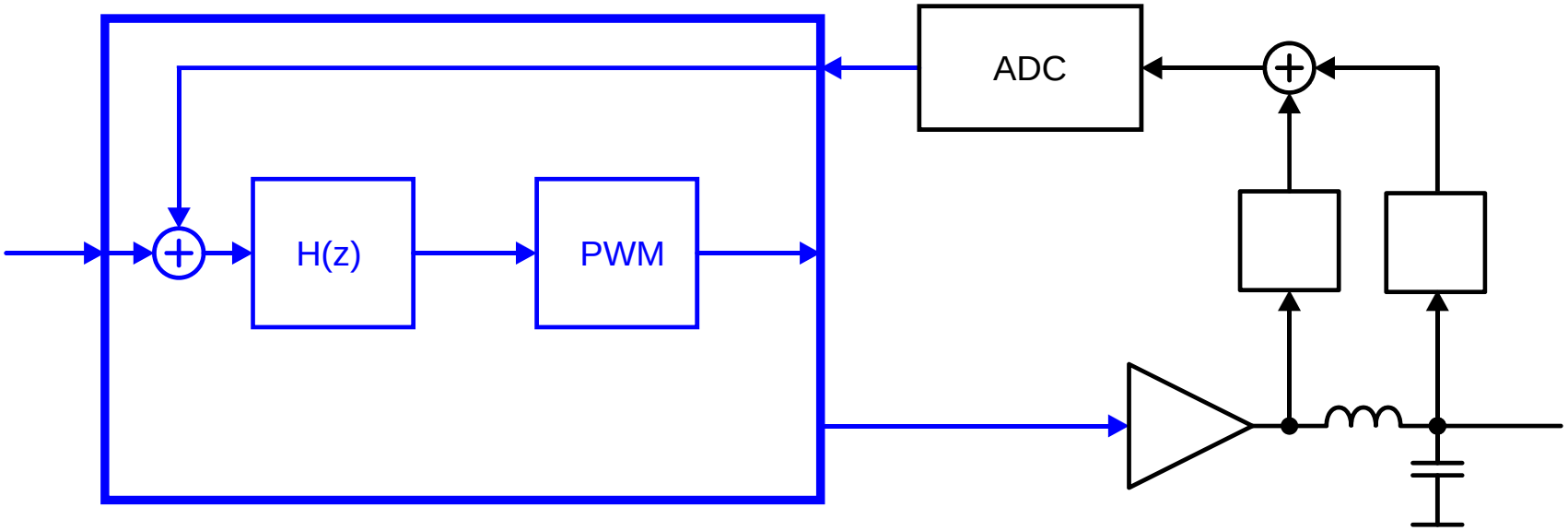


Rearranged loops

...a remarkable similarity...



Full ADC based feedback



Full ADC based feedback

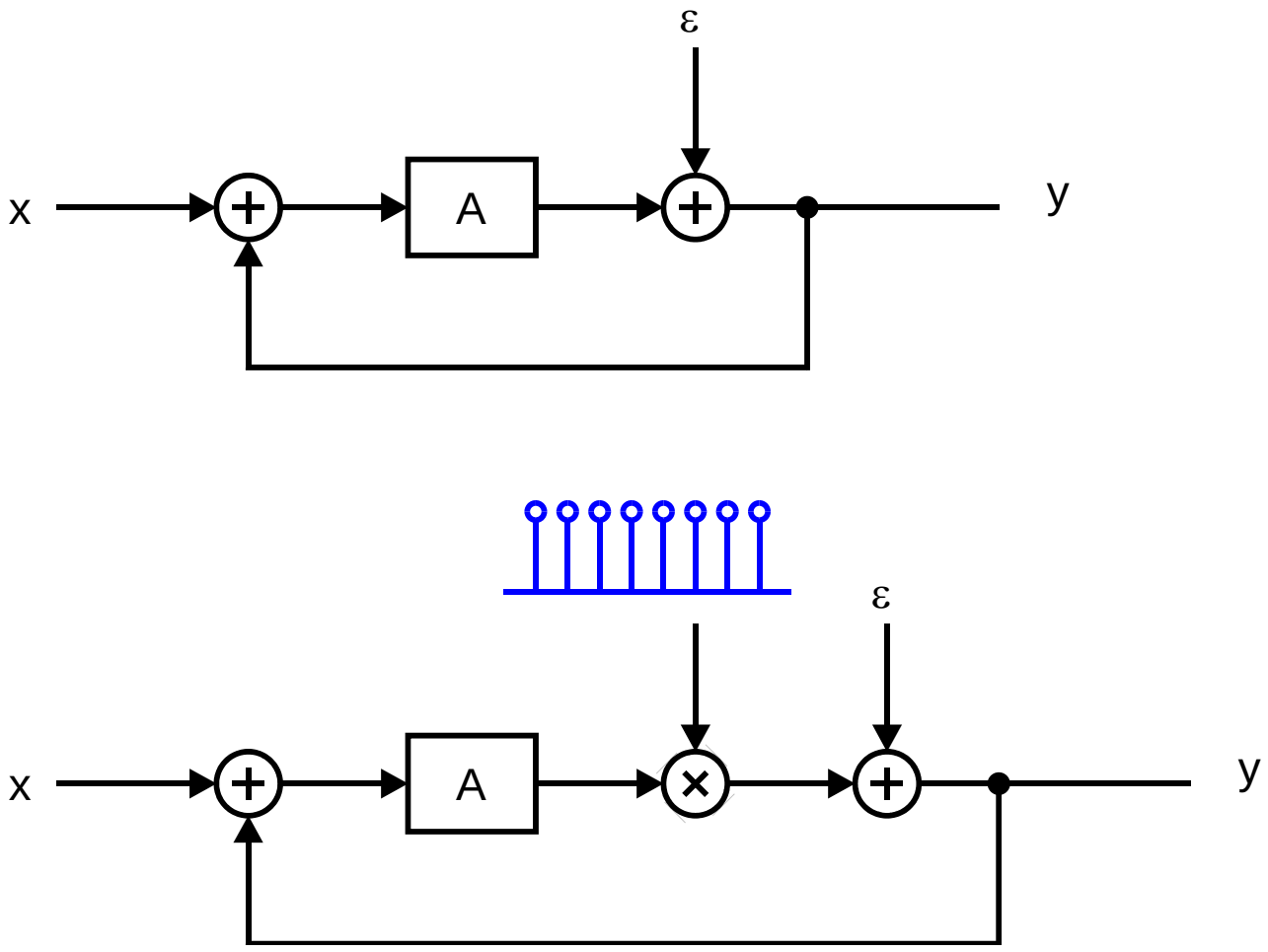
Reasons for use

- Silicon area of ADC + loop control < equivalent analogue loop.
- Complicated linearization circuits
- Start/stop/overload recovery

Not reasons for use

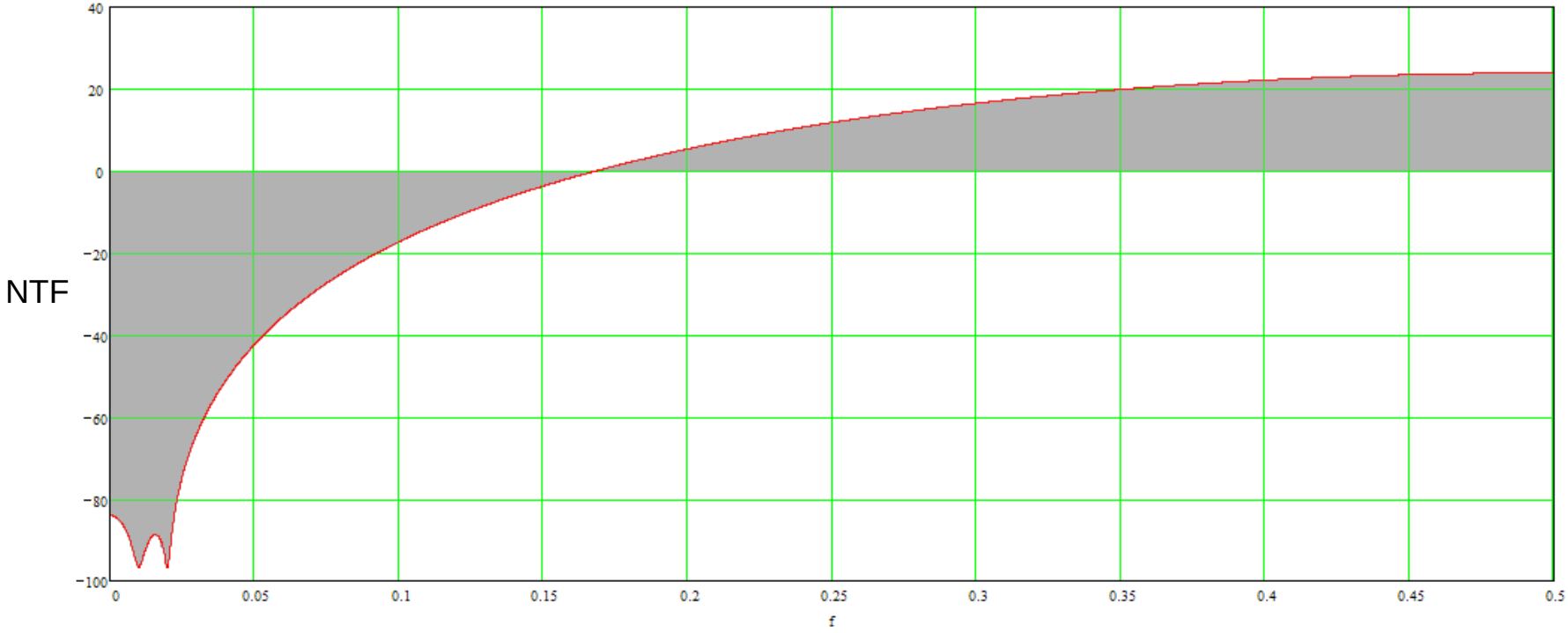
- Nearly anything else:
  - “digital, hence better”
  - investor retention

Effect of sampling on loop control



Effect of sampling on loop control

Noise Shaper Theorem holds

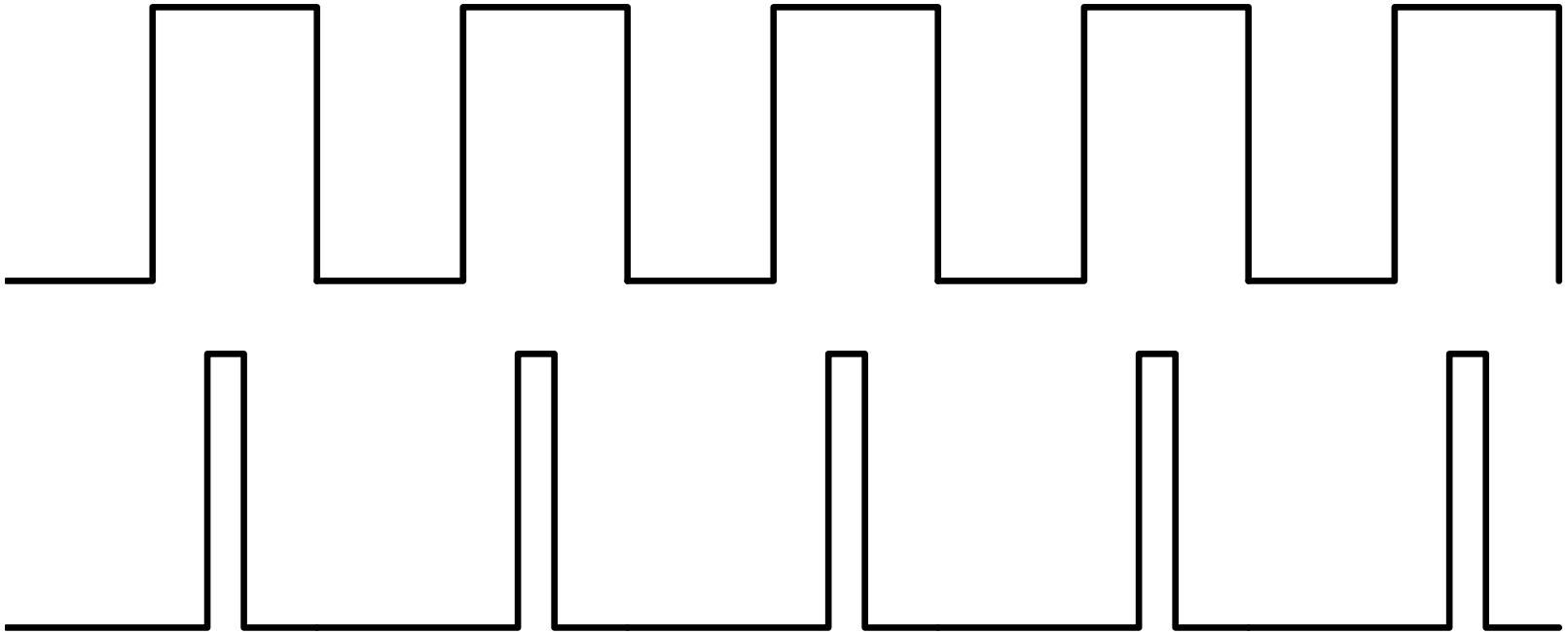


- Transform A_L to z domain
- Highly optimised A_L may seem instable in linear analysis and be critically damped in sampled system!

Effect of sampling on loop control

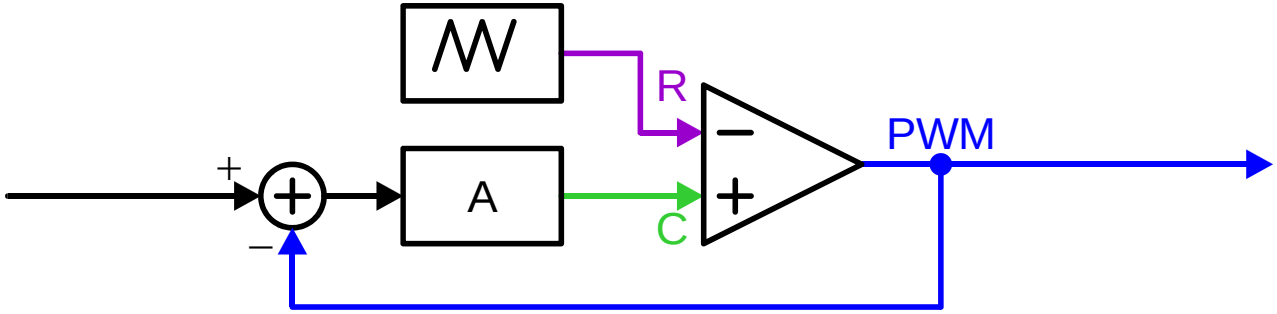
Most PWM is double-sided

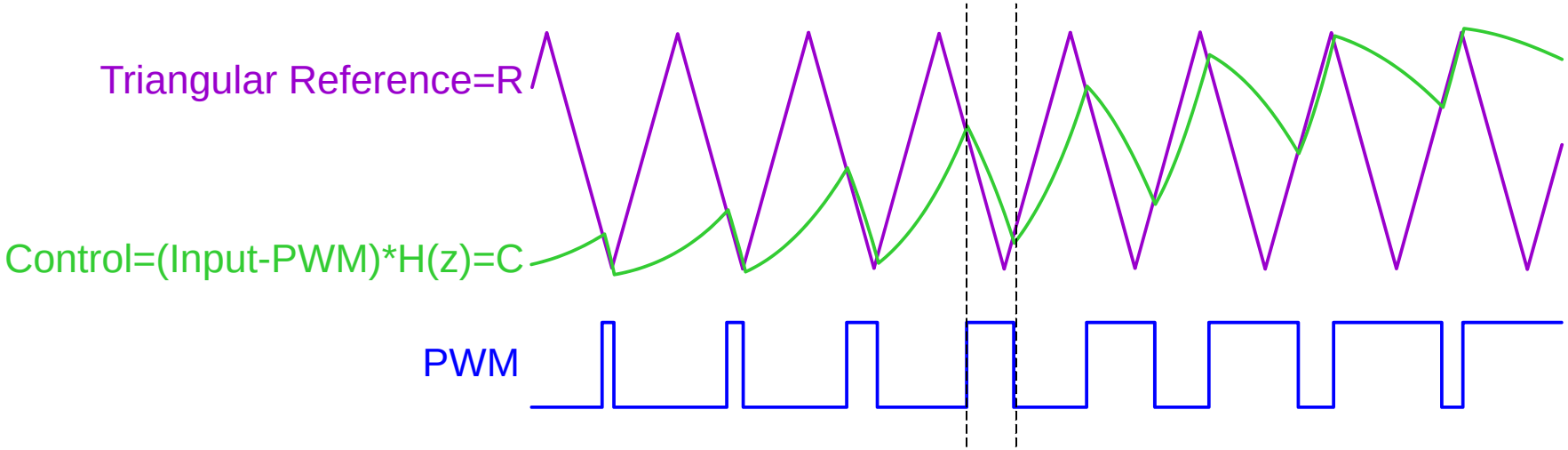
- $f_s = f_{sw}$ (low modulation index)
- $f_s = 0.5 \cdot f_{sw}$ (clipping)



- ETF (NTF) becomes modulation dependent

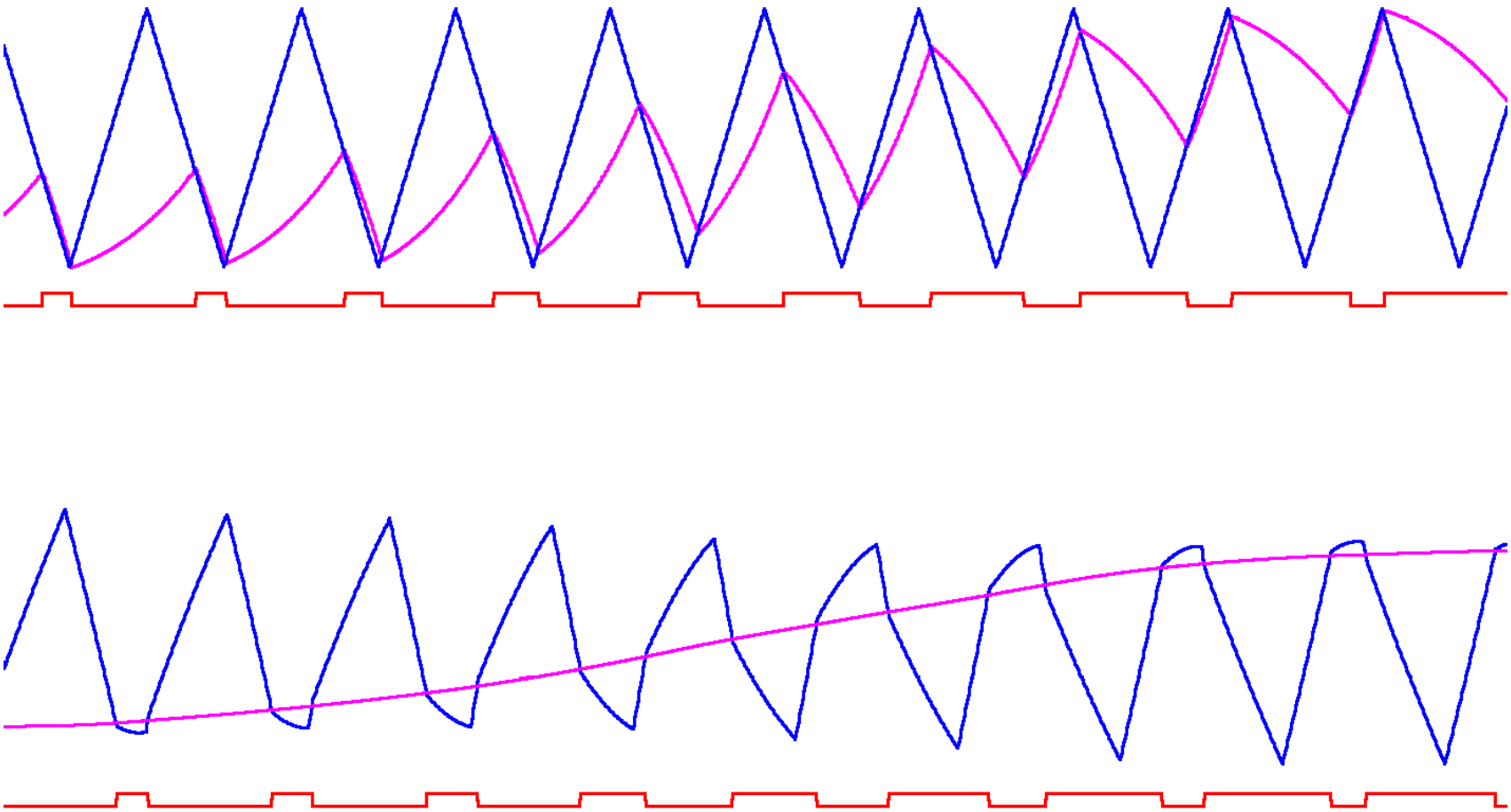
Ripple aliasing





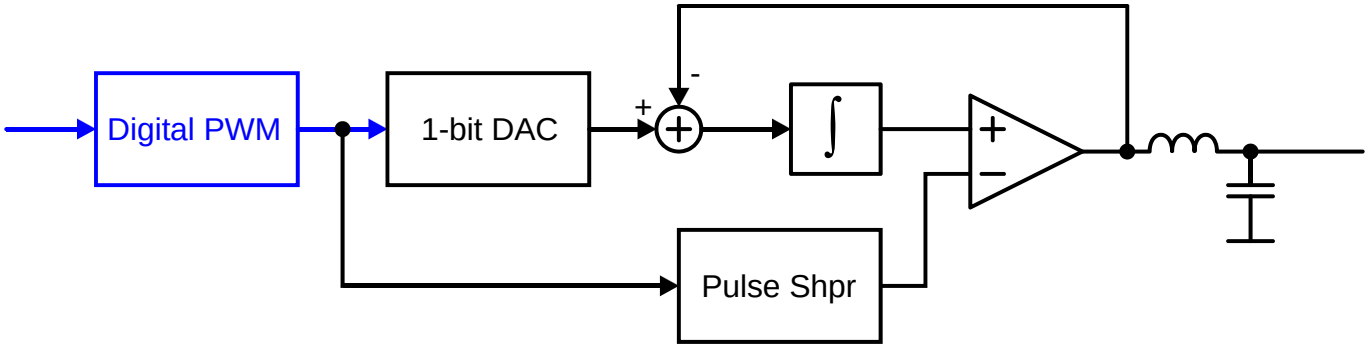
Ripple aliasing

Ripple distorts carrier



Dealing with Ripple Aliasing

Local Error Feedback (PEDEC etc)



- Operation
  - Minimal ripple in feedback loop.
- Pro
  - Theoretically perfect regardless of loop order
- Contra
  - Gains must be matched: 1-bit DAC and PWM must scale with supply
  - PWM generator is a problem in its own right
  - Not compatible with post-filter feedback

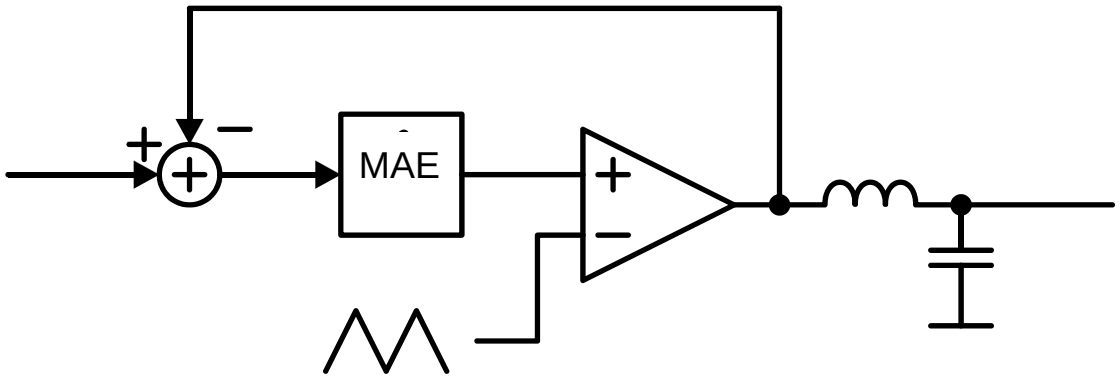
Dealing with Ripple Aliasing

Carrier slope correction (Candy)

- Operation
  - Dynamically modify triangle wave slopes
- Pro
  - Theoretically perfect for 1st order loop
  - Reasonably compatible with higher order including mixed post-filter f/b
- Contra
  - Complex triwave generation

Dealing with Ripple Aliasing

Minimum Aliasing Error filter (Risbo)



- Operation
  - Ripple in feedback loop not reduced, phase shift optimised for minimum impact.
- Pro
  - Grafts well onto “standard” control circuit.
  - Compatible with post-filter feedback (perhaps not fully global)

Dealing with Ripple Aliasing

“Invariant PWM” (Yours Truly)

- Operation
  - Secret
- Pro
  - Perfectible for any loop (5th order with global f/b demonstrated)
  - Compatible with global f/b
  - Closed-form analysis and design
- Contra
  - Complex triwave generation
  - High sensitivity to parts tolerance

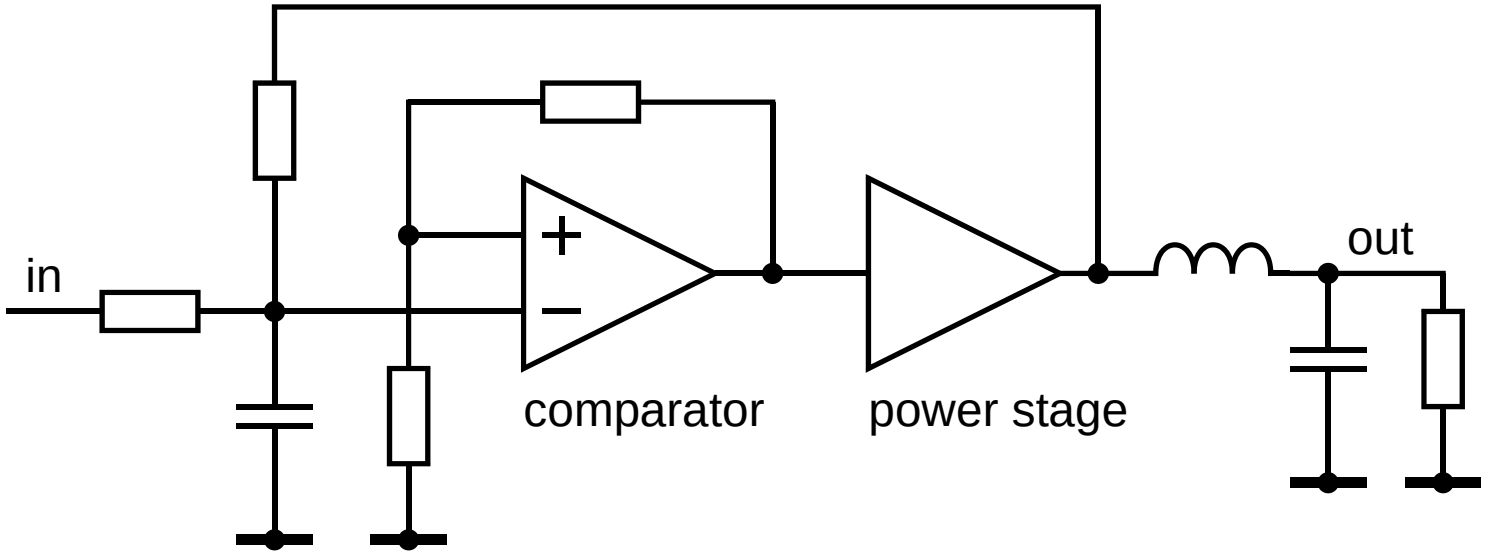
Self-Oscillating Loops

Aim

- Getting rid of the oscillator
- Improving maximum modulation index

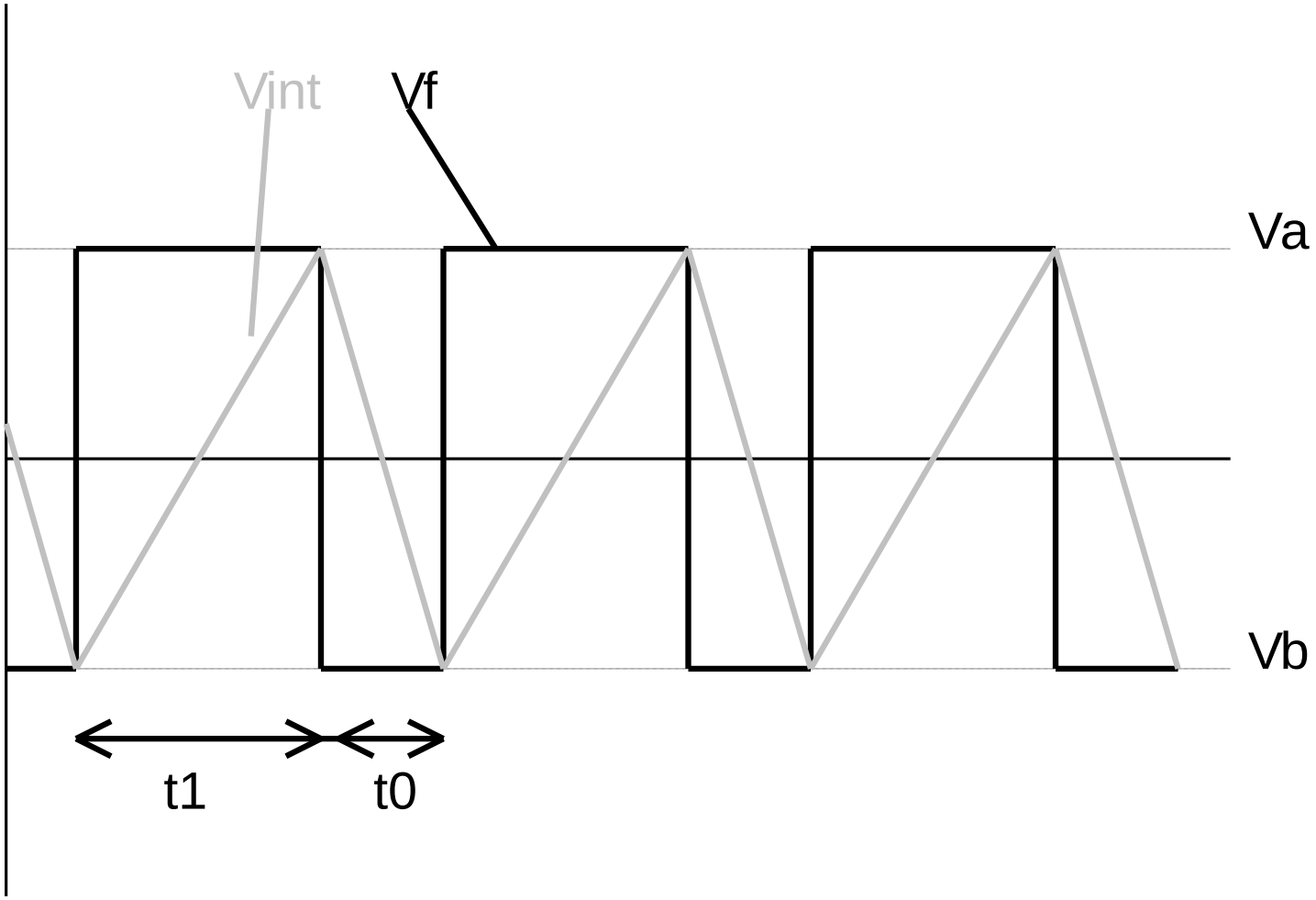
Self-Oscillating Loops

Hysteresis modulator



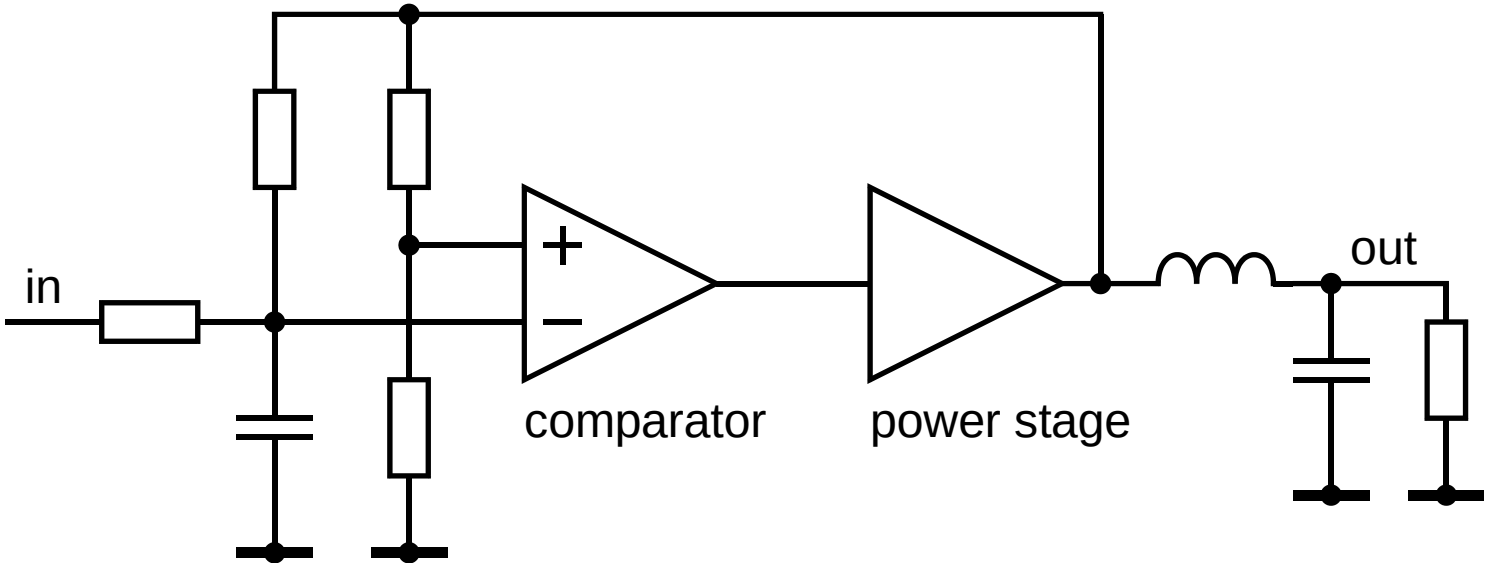
Hysteresis modulator

Operation



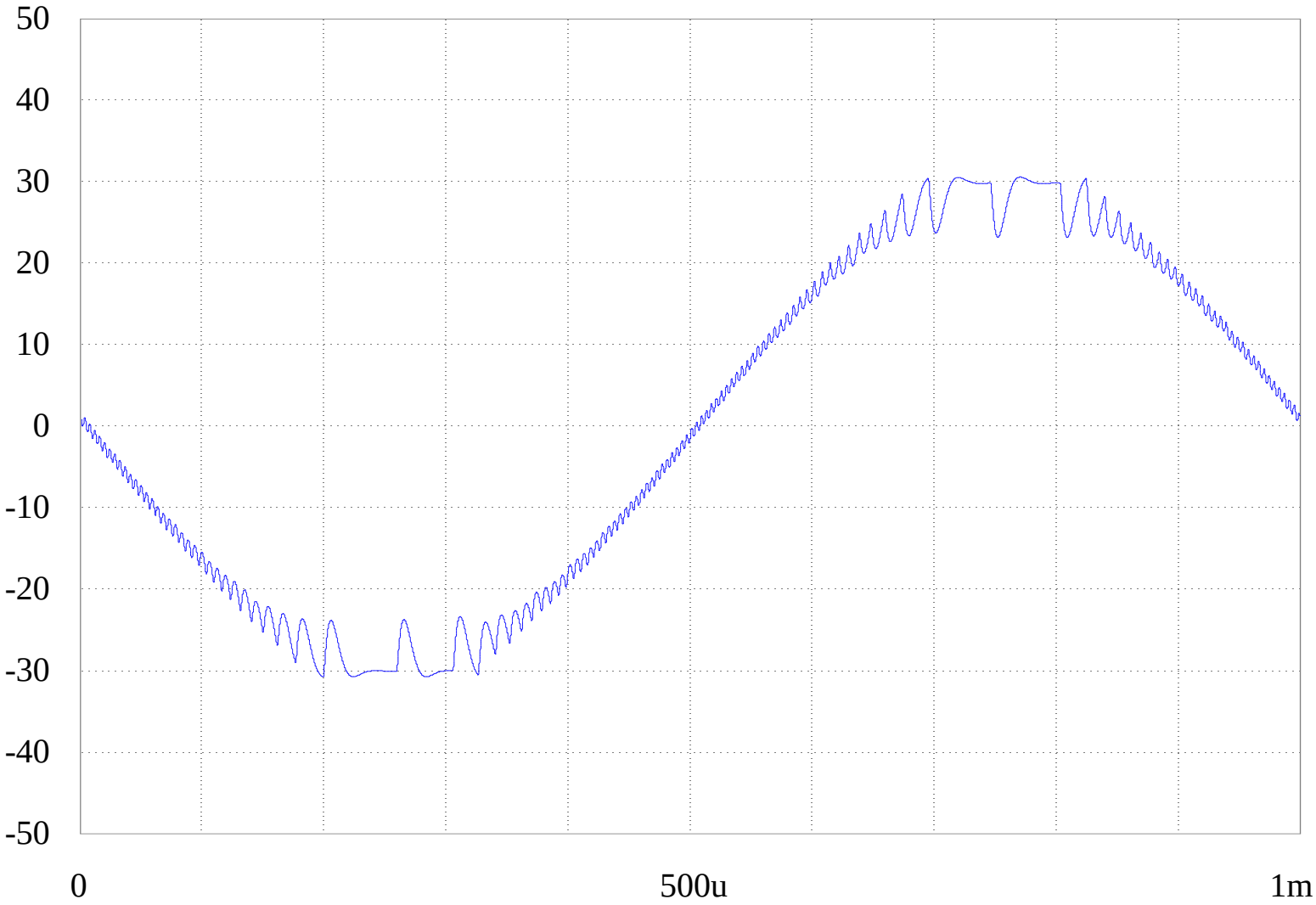
Hysteresis modulator

Improved version



Hysteresis modulator

Output Signal

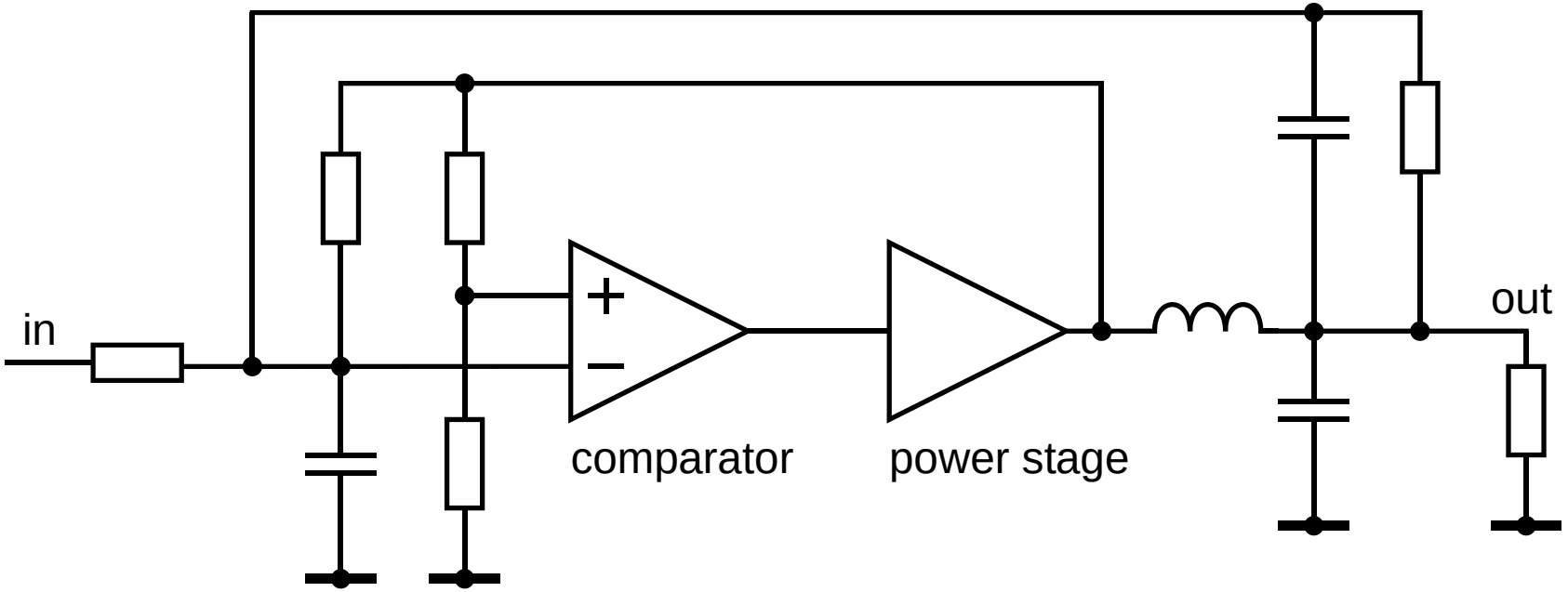


Hysteresis modulator

- Completely linear
- Switching frequency falls early
  - becomes audible near clip

Hysteresis modulator

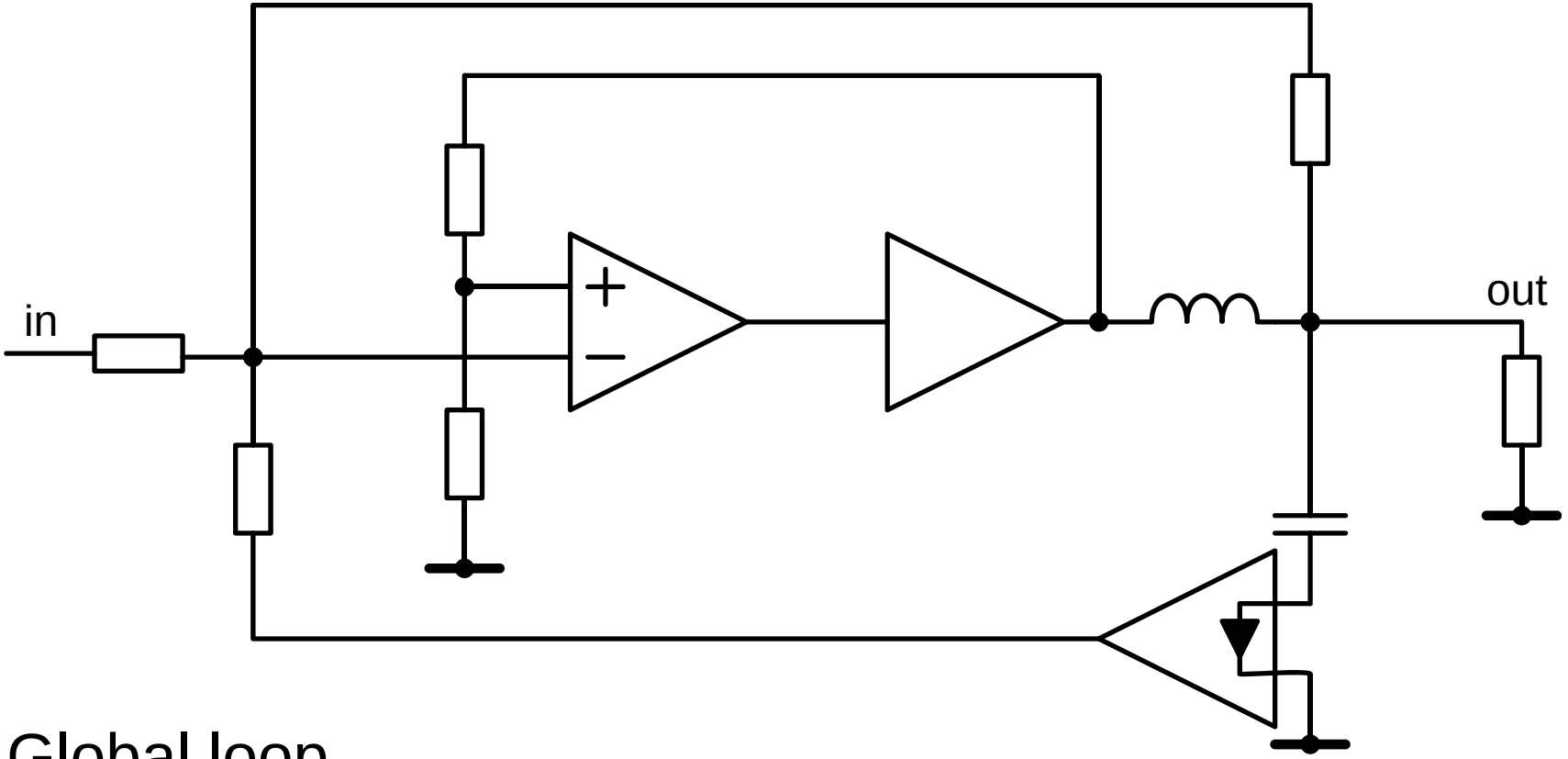
Post-LPF added



- Less linear
- No-load stability not guaranteed

Hysteresis modulator

Capacitor current feedback (Mueta)

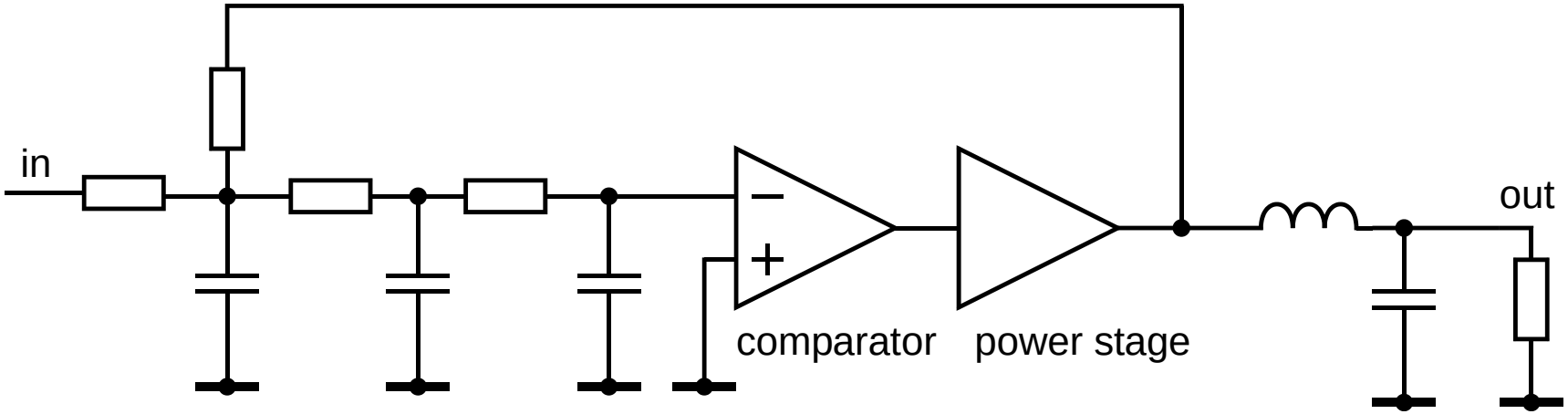


- Global loop
- Good linearity
- Current sense has low EMI sensitivity

Phase-shift controlled oscillation

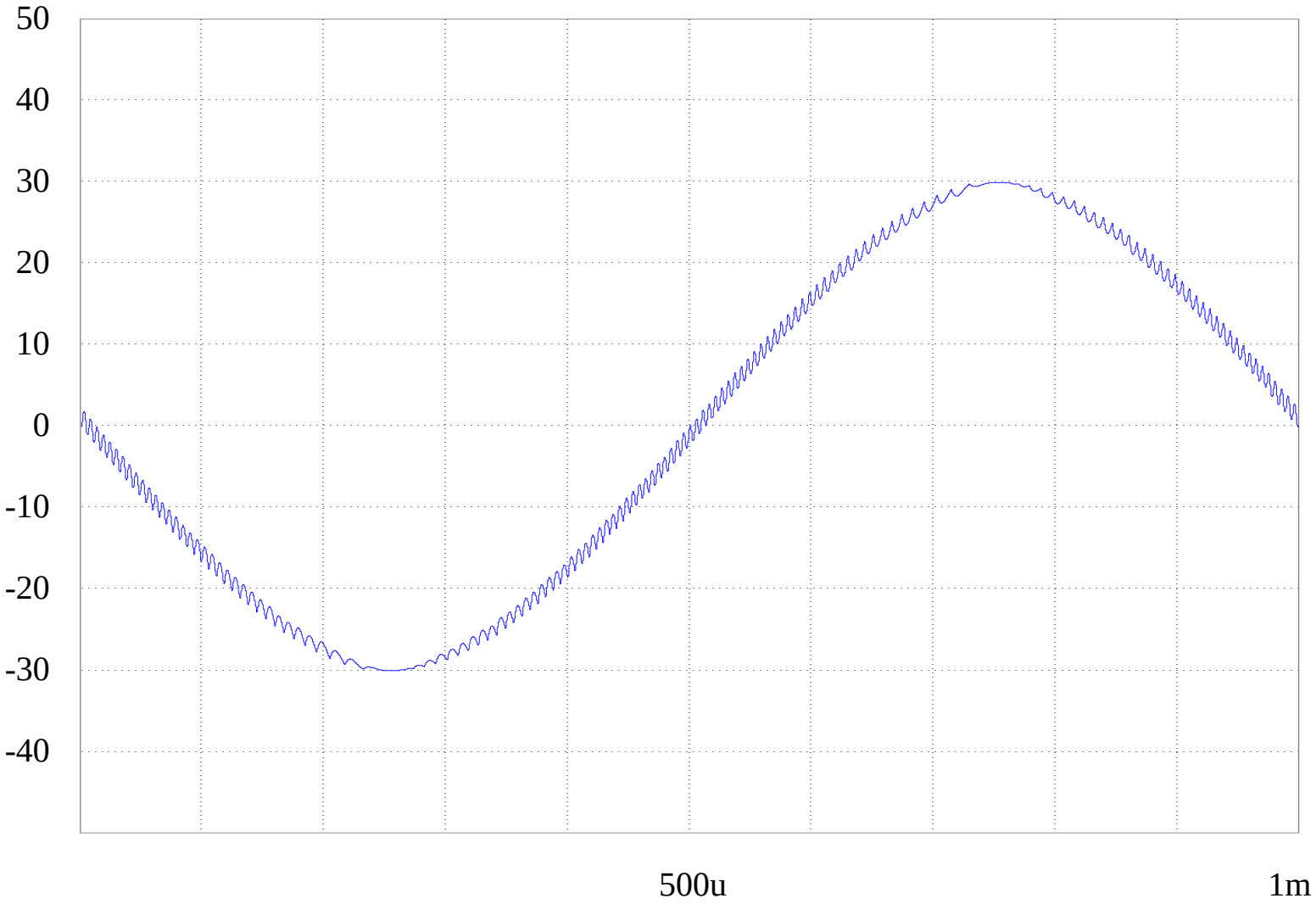
Operation

- Oscillation frequency set by loop phase



Phase-shift controlled oscillation

Output signal

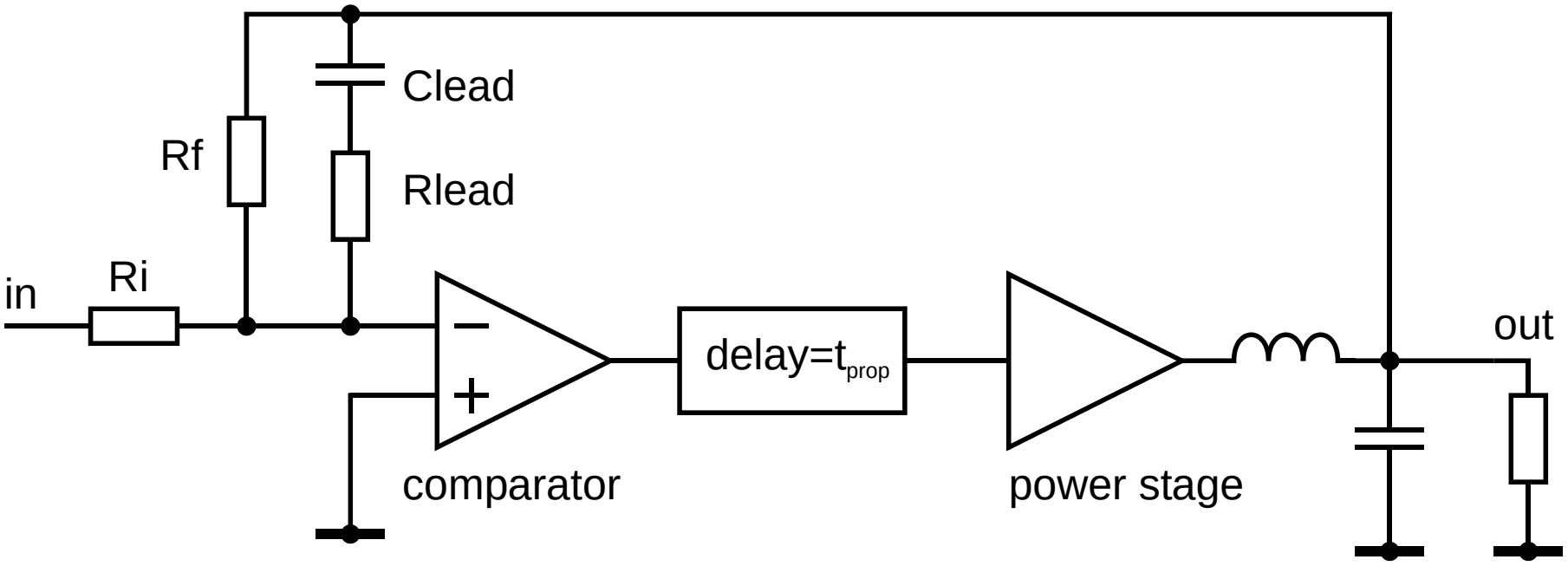


Phase-shift controlled oscillation

- Nonlinear, depends on design
- Switching frequency is more stable

Phase-shift controlled oscillation

Phase shift controlled oscillator with global loop (UcD)

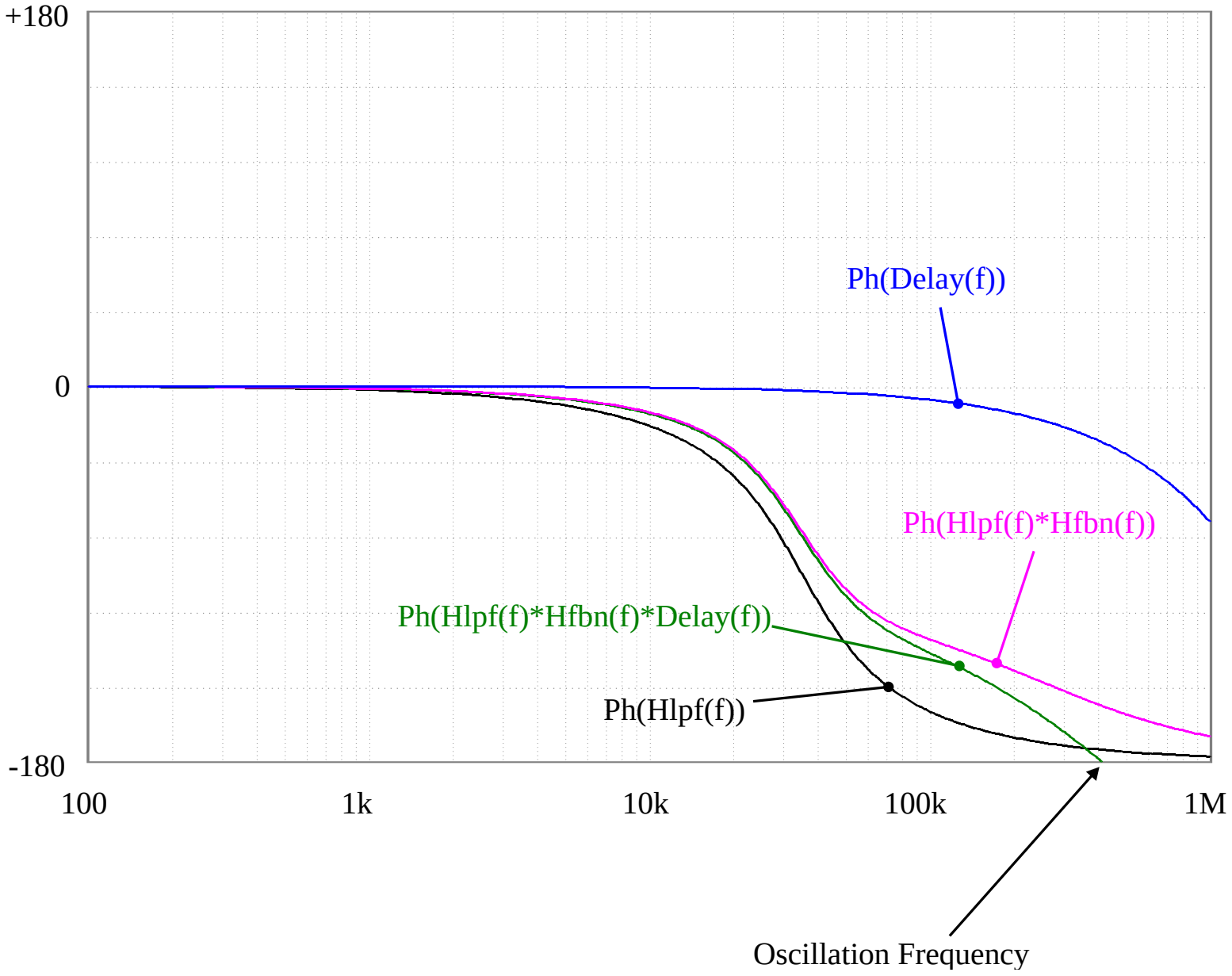


UcD

Operation

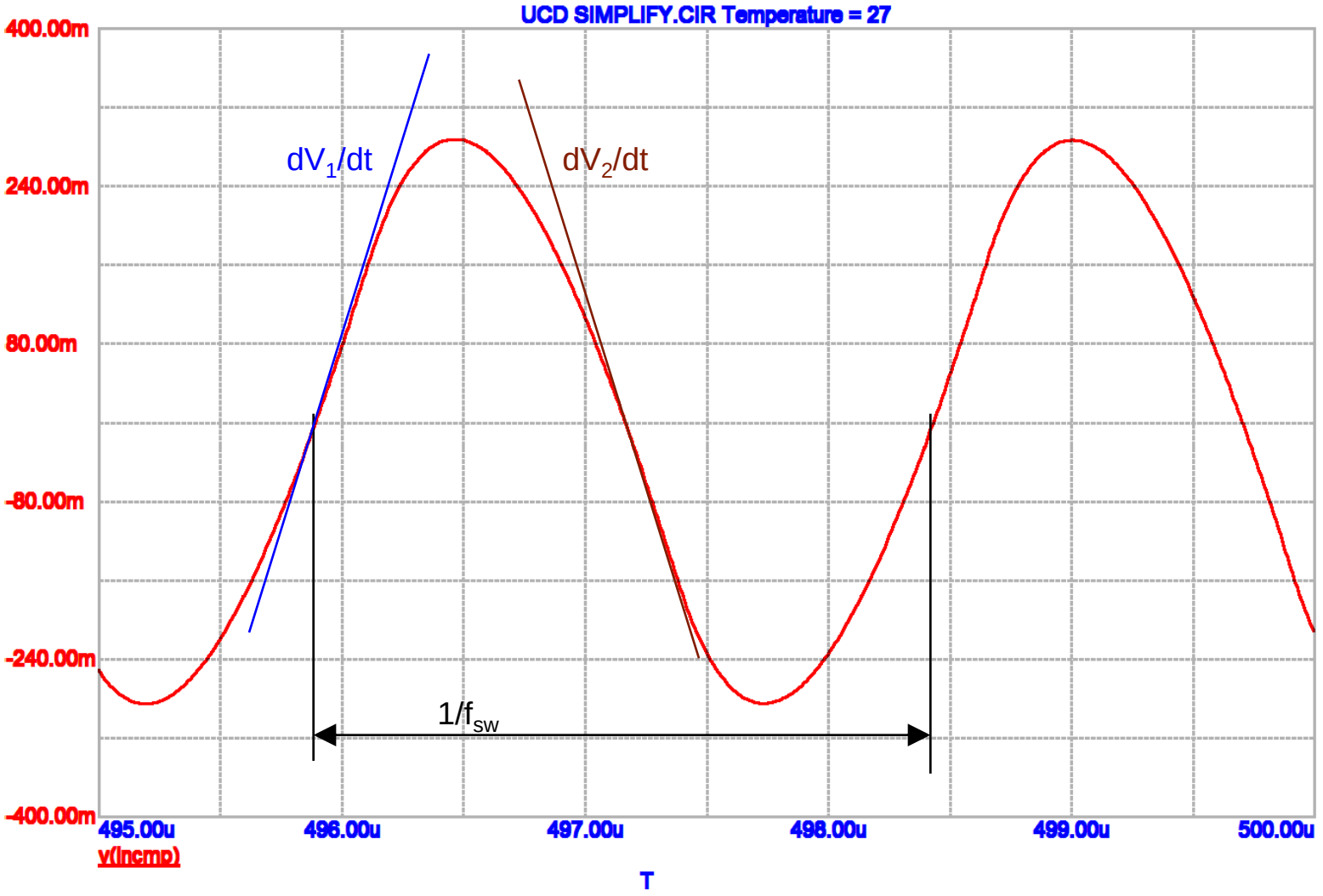
- Combined phase shift of output filter, lead network and propagation delay set f_{osc}.
- Extra pole may be added

UcD


+180
0
-180
100
1k
10k
100k
1M
Ph(Delay(f))
Ph(Hlpf(f)*Hfbn(f))
Ph(Hlpf(f)*Hfbn(f)*Delay(f))
Ph(Hlpf(f))
Oscillation Frequency

Phase-shift controlled oscillation

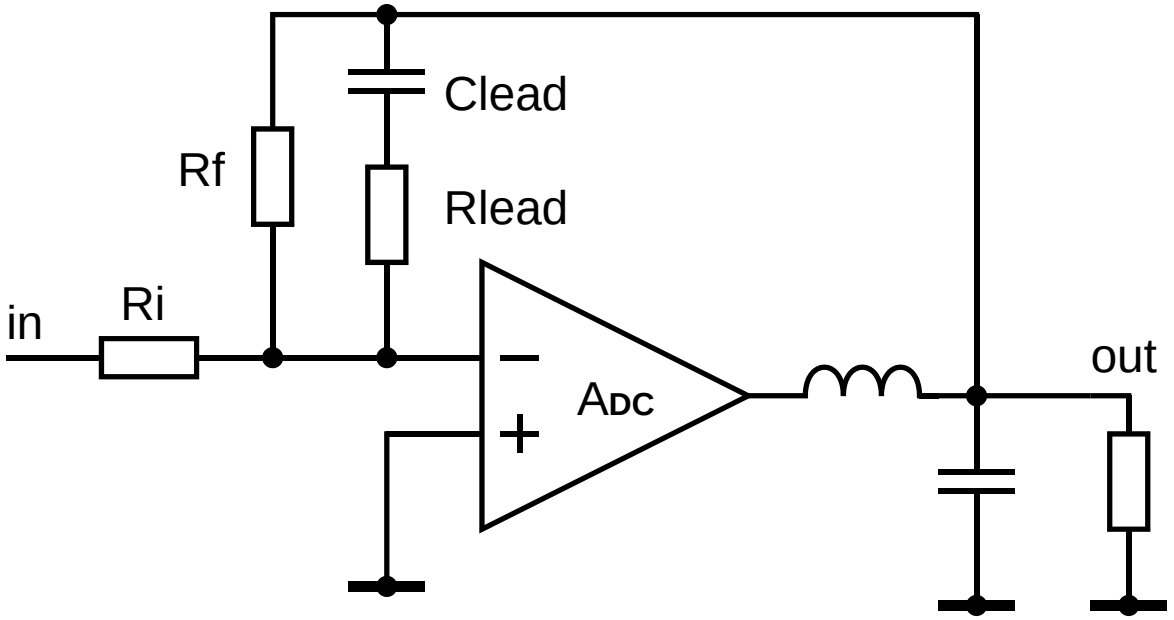
Modulator gain



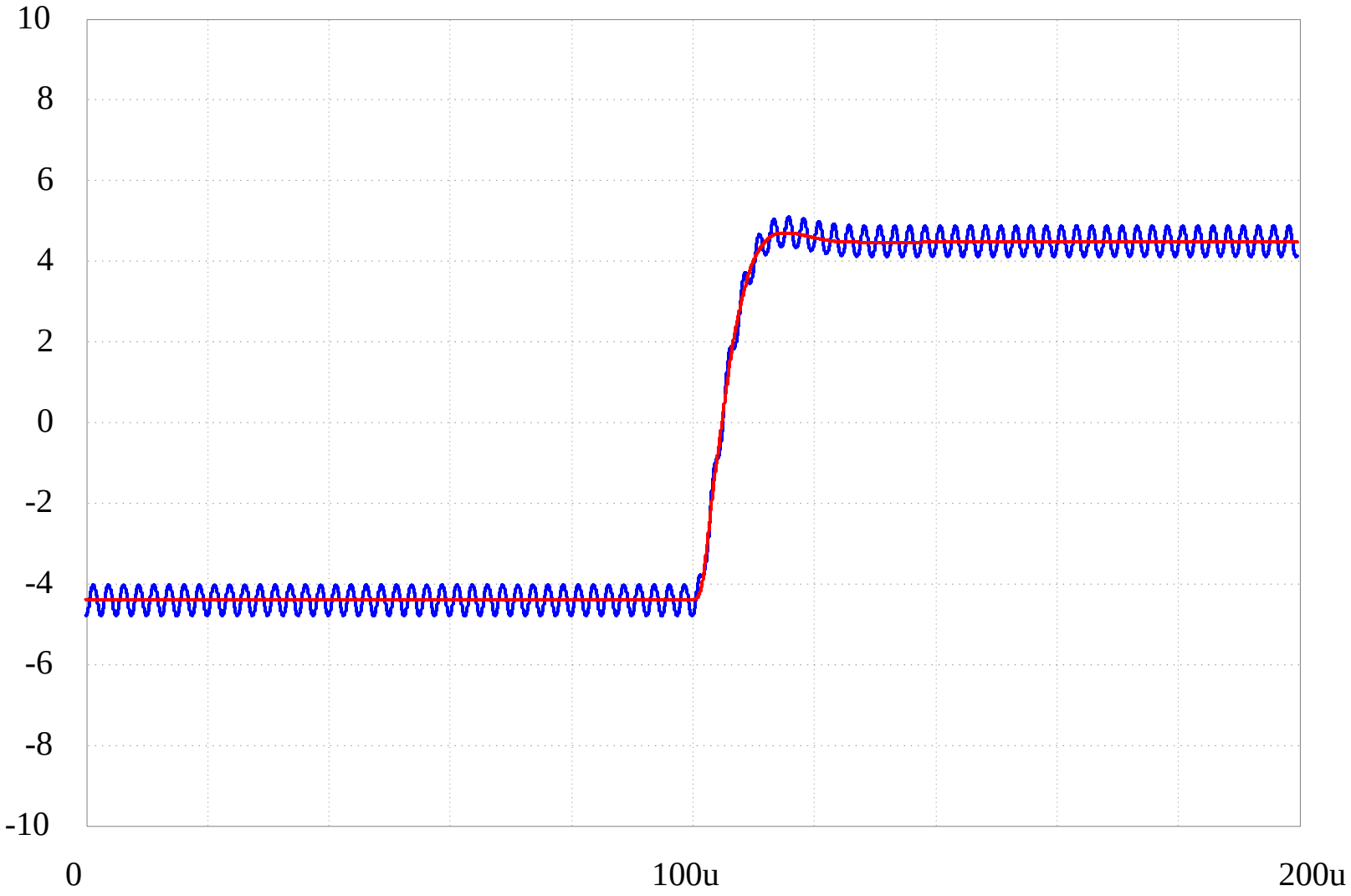
Phase-shift controlled oscillation

Small-signal linearized model

$$A_{DC} = 2 \cdot V_{CC} \cdot f_{sw} \cdot \left(\frac{1}{\frac{dV1}{dt}} - \frac{1}{\frac{dV2}{dt}} \right)$$



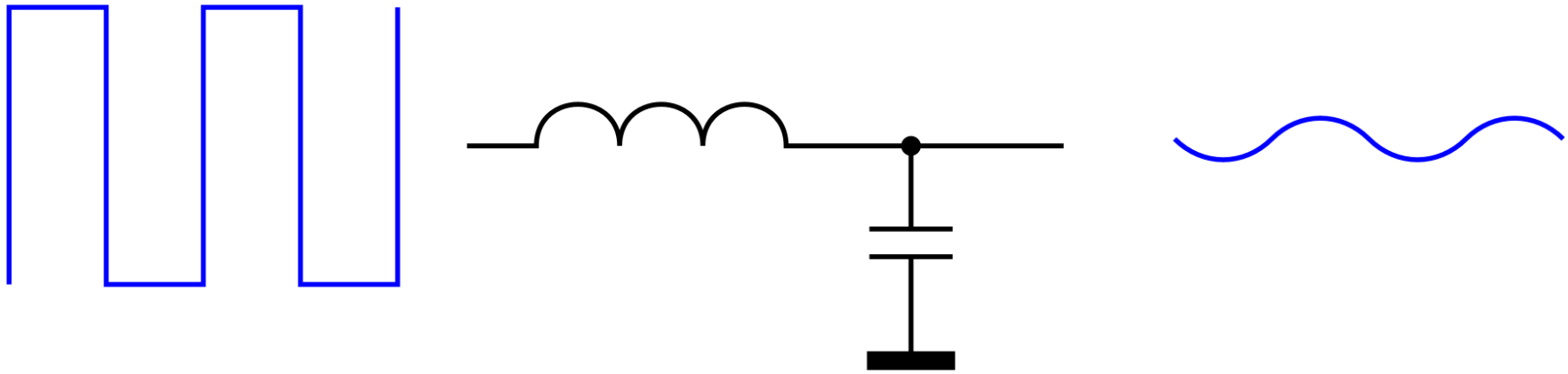
Phase-shift controlled oscillation



Class D and EMI

Low-frequency EMI: Carrier and low harmonics.

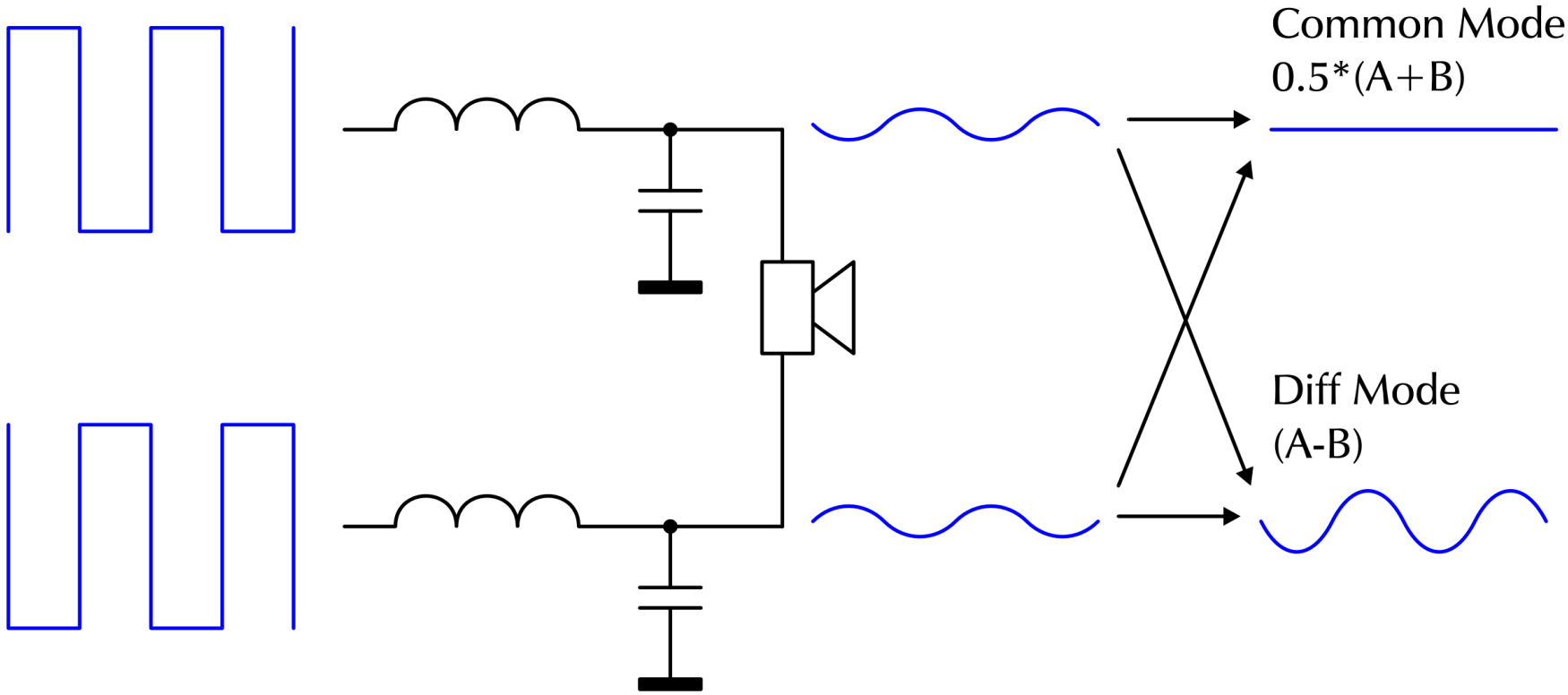
- Close match with theory.
- Ripple cancelling possible.
- Not an EMI issue except for long cables
- Not a tweeter issue (come off it!)



Class D and EMI

Common and Differential Mode in H-Bridge Class D

- “Class AD”. Carriers and modulation are out of phase

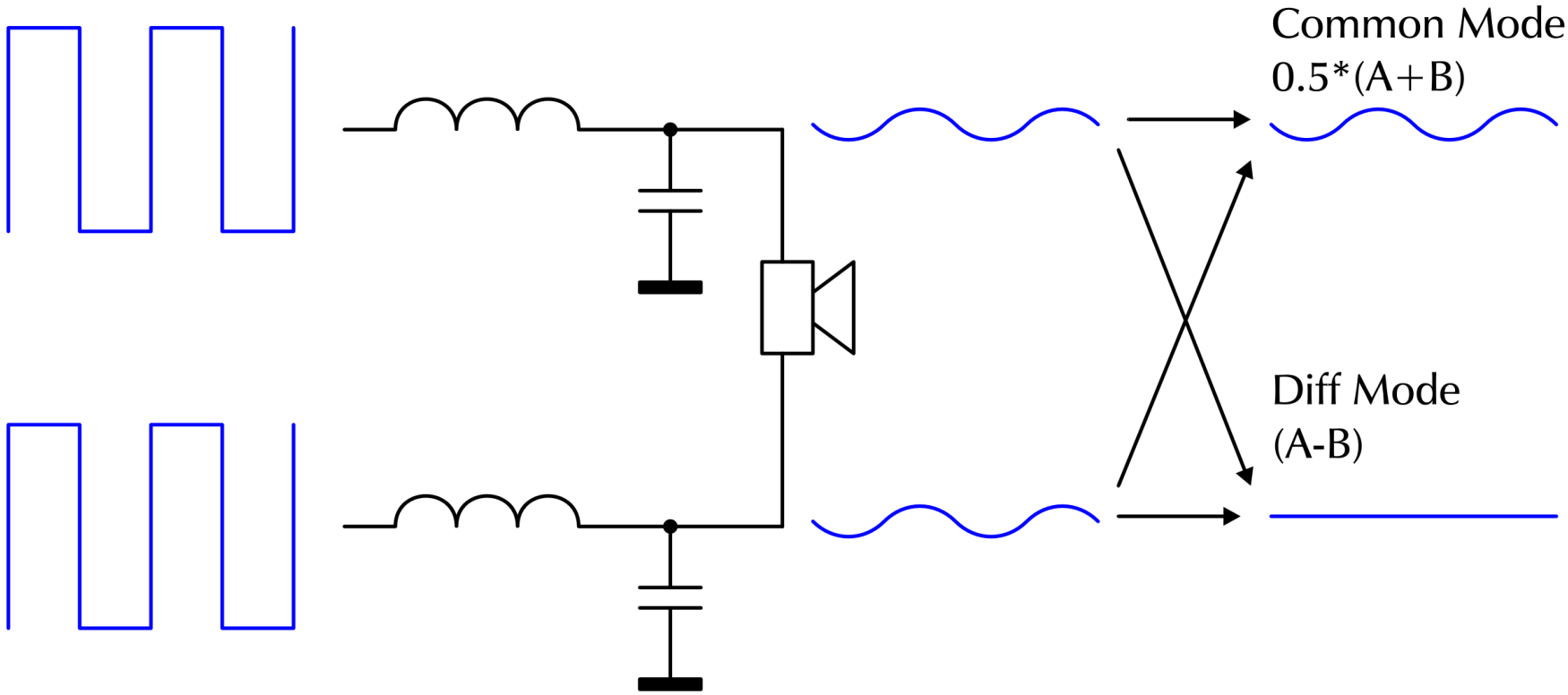


Note: Common-mode is what radiates off cables.

Class D and EMI

"Class BD".

- Carriers are in phase. Modulation is out of phase.



HF across load is reduced but CM increases.

Class D and EMI

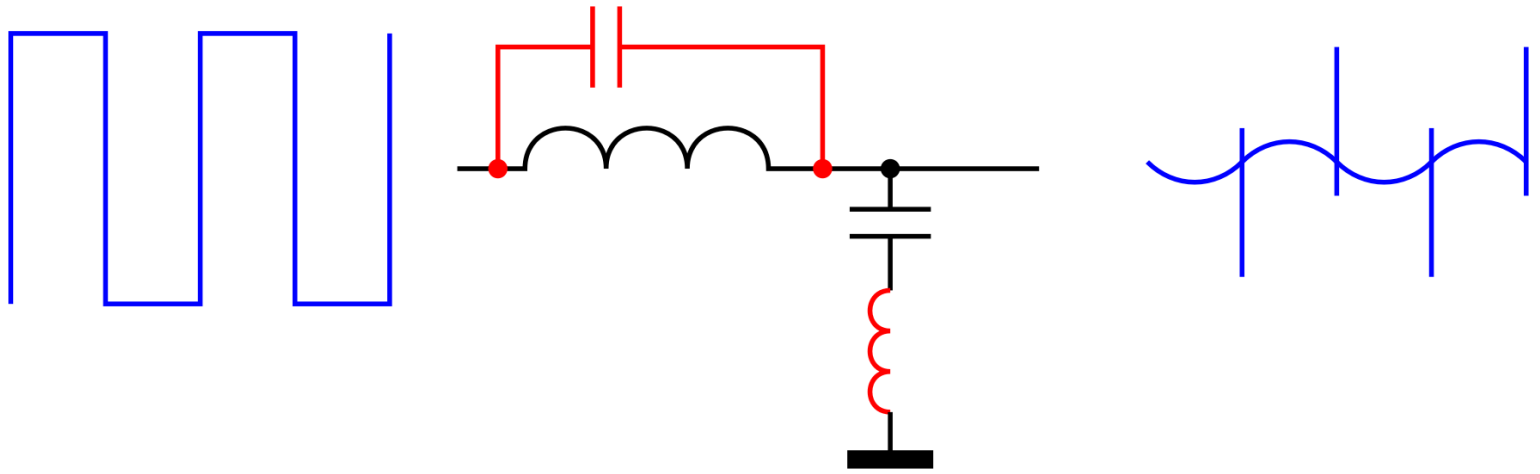
Half bridge vs Full Bridge, Class AD vs BD

- Half-bridge
  - Can’t cancel either CM or DM
  - Common-mode is half of differential mode
- AD
  - Common-mode voltage theoretically 0
  - Differential mode same as half bridge
- BD
  - Differential mode cancels at low modulation...
    ...but that was not really a problem anyway.
  - Common-mode voltage same as half bridge

Class D and EMI

High-Frequency EMI: Leaking switching transients

- Theoretical modeling is useless.
  - Capacitors become inductive
  - Inductors become capacitive
  - PCB becomes jumble of L's and C's.
- No tricks. Only good hardware design helps.
- Direct EMI problem under all circumstances.



Class D and EMI

Sensitive item 1: The capacitor.

- Myth of the “Low Inductance Capacitor”. (An Audiophile Favourite)
  - All modern film caps have sprayed end contacts.
  - Inductance is determined by geometry only (mostly size).

Bad.

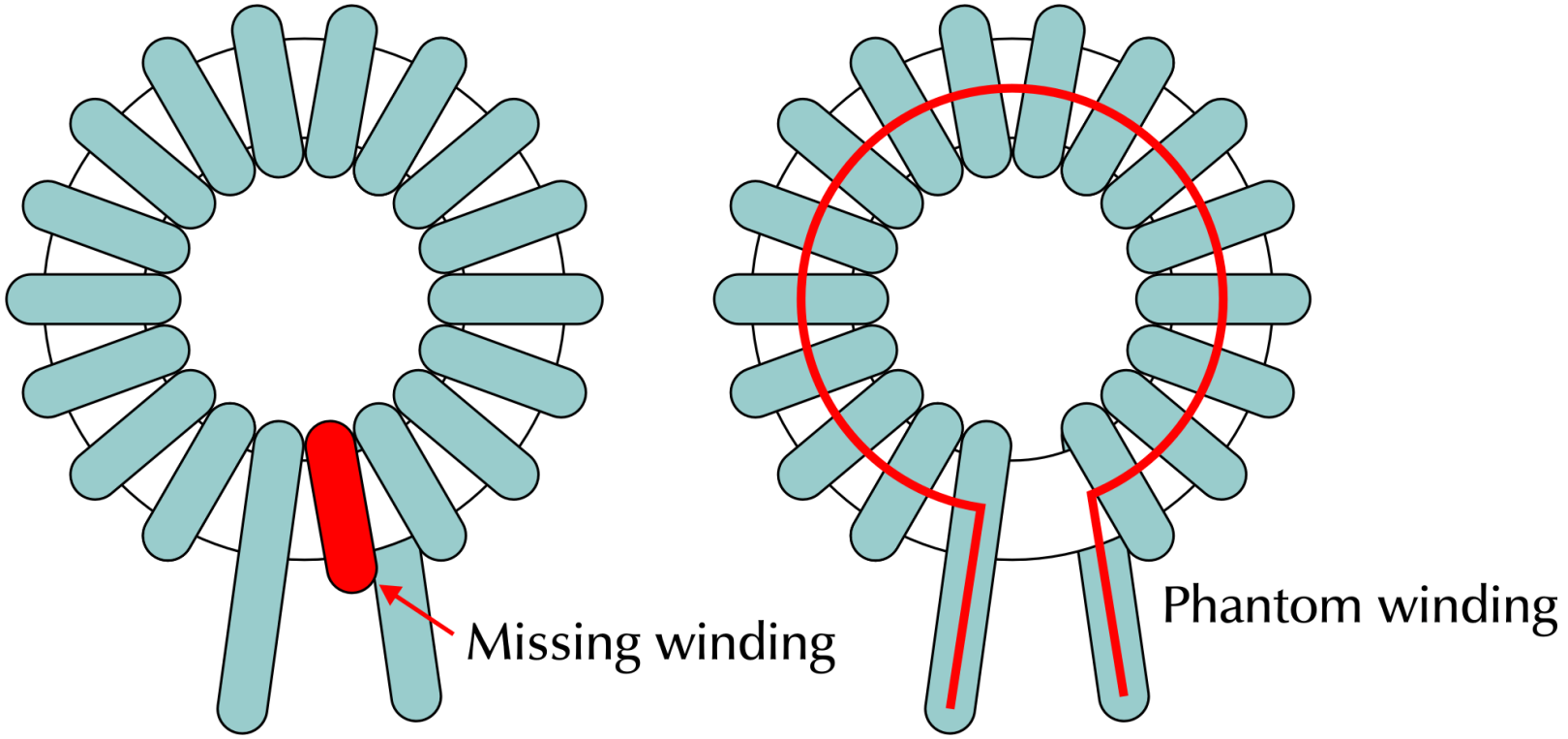
Good.

Period.

Class D and EMI

Sensitive item 2: The inductor.

- Stray fields out of toroids

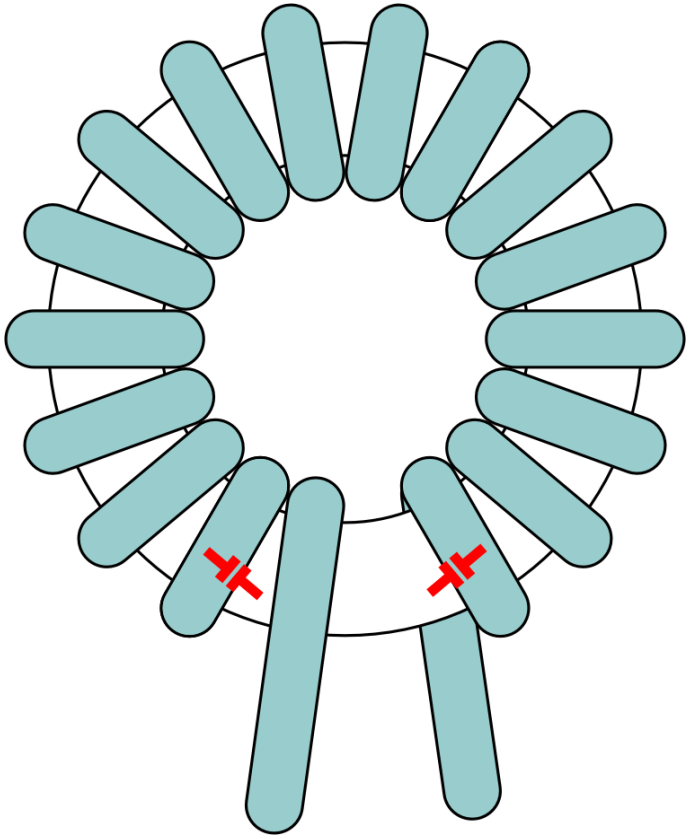


- Upright mounted toroids are worst.

Class D and EMI

Sensitive item 2: The inductor.

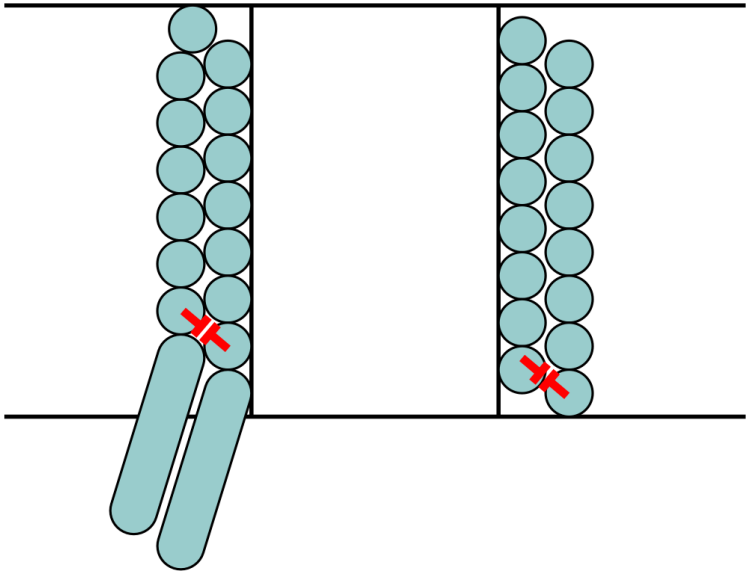
- Beware of indirect Capacitive Coupling through Core
  - Tight windings are better magnetically but worse electrostatically.
  - No external electrostatic shield: Capacitive coupling to chassis etc. can get significant.
- Toroids are not always optimal



Class D and EMI

Sensitive item 2: The inductor.

- Ferrite inductors: avoid direct capacitive coupling between windings

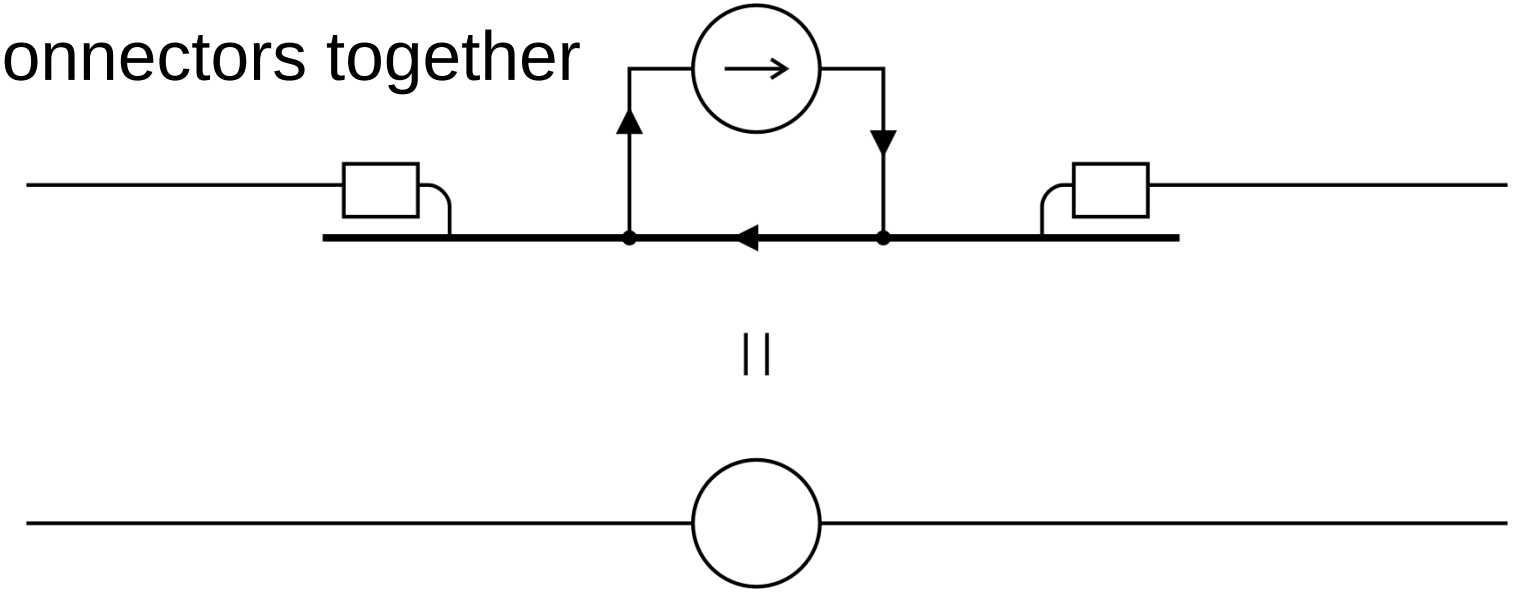


- “Hot” end sees “Cold” end
- 2 layers is worst case situation
- 1 layer is best

Class D and EMI

Sensitive item 3: The PCB layout.

- Contiguous ground plane
- Keep connectors together



- Avoid capacitive coupling to external parts
- Minimize loop area (≠short traces)

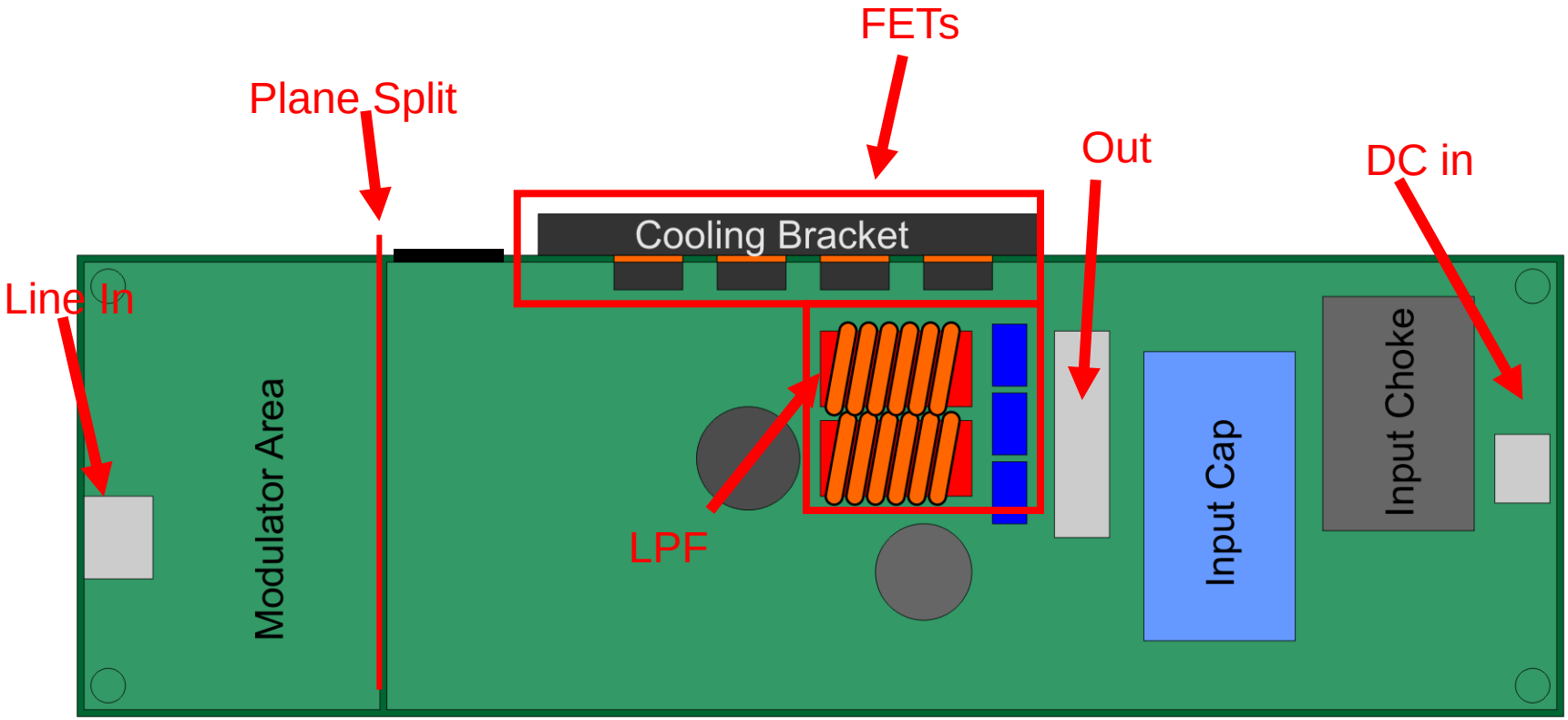
Class D and EMI

Checking for EMI without Spectrum Analyser

- Just probe around the external connections with a scope!!!
- If you see rubbish, there is rubbish
- The higher the frequency, the more you should worry

Class D and EMI

Example: Amplifier A, rated 160W

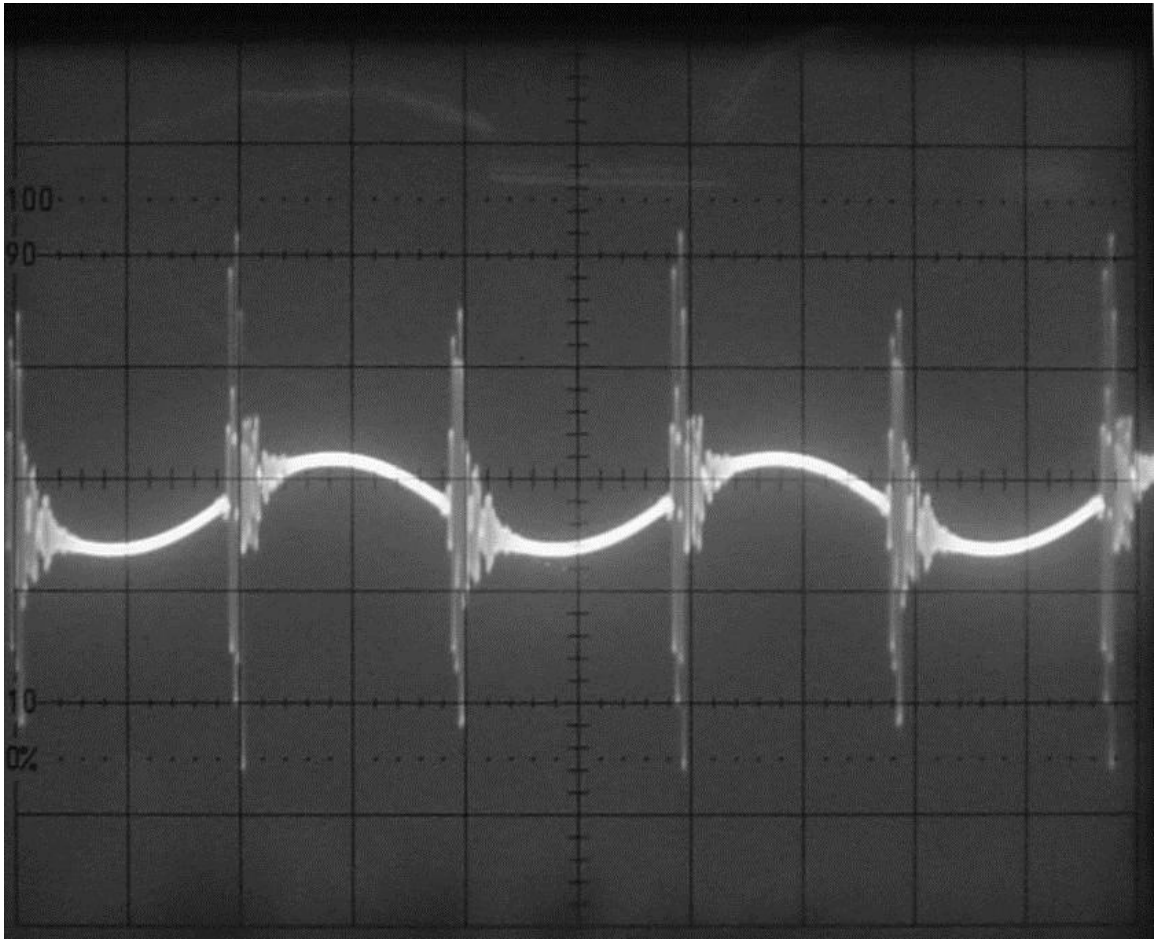


(sketch of circuit board found in commercially available amp)

Class D and EMI

Amplifier A, one output line

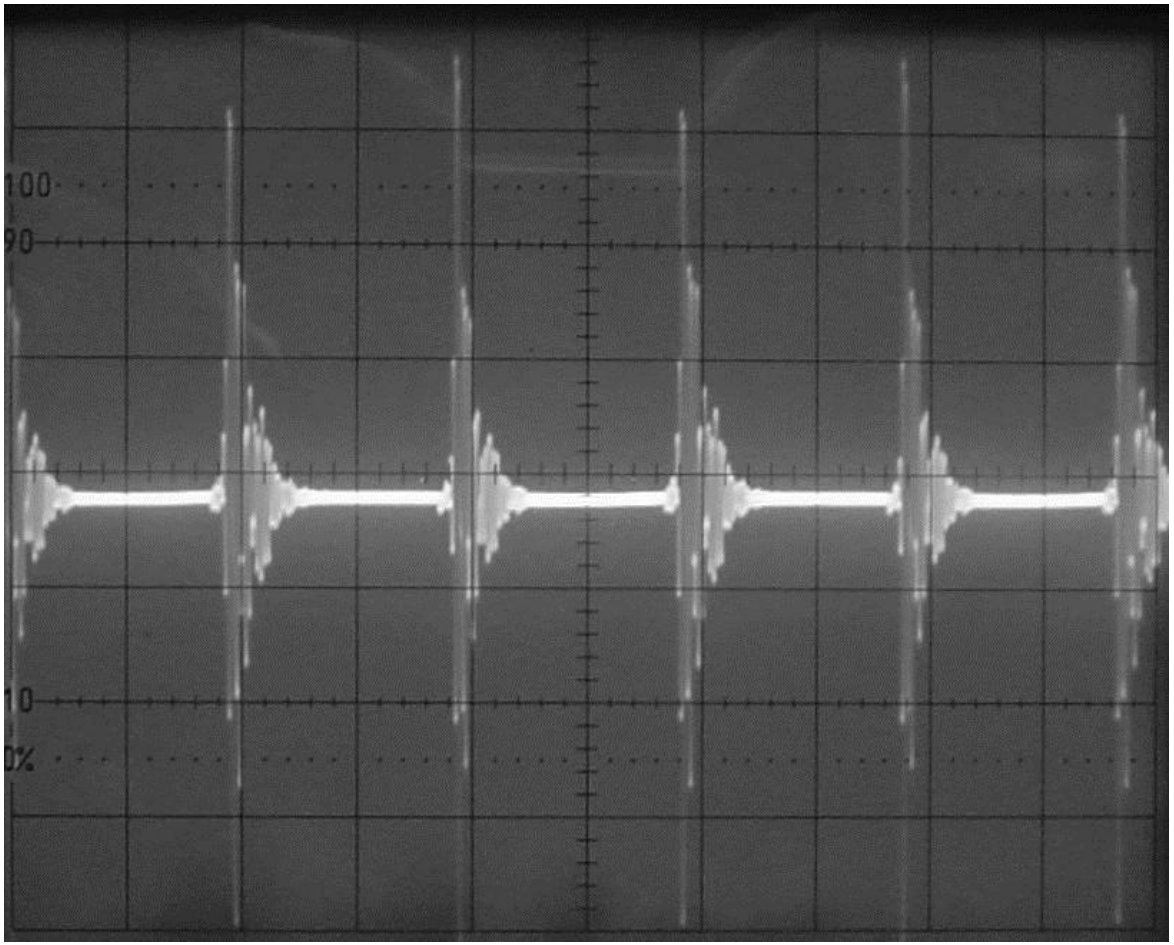
- 1V/div. Probe clip at RCA ground.



Class D and EMI

Amplifier A, common mode

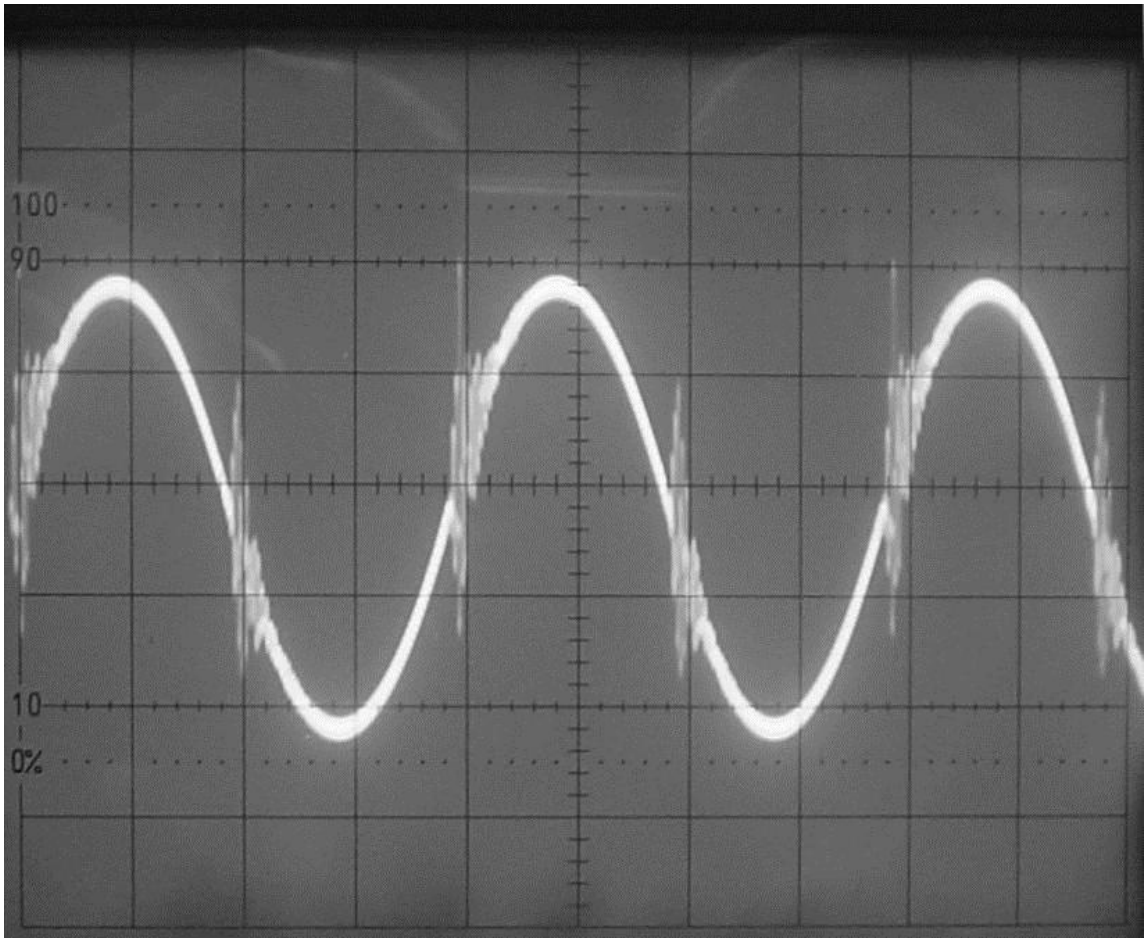
- 500mV/div. Amp is claimed to pass FCC???



Class D and EMI

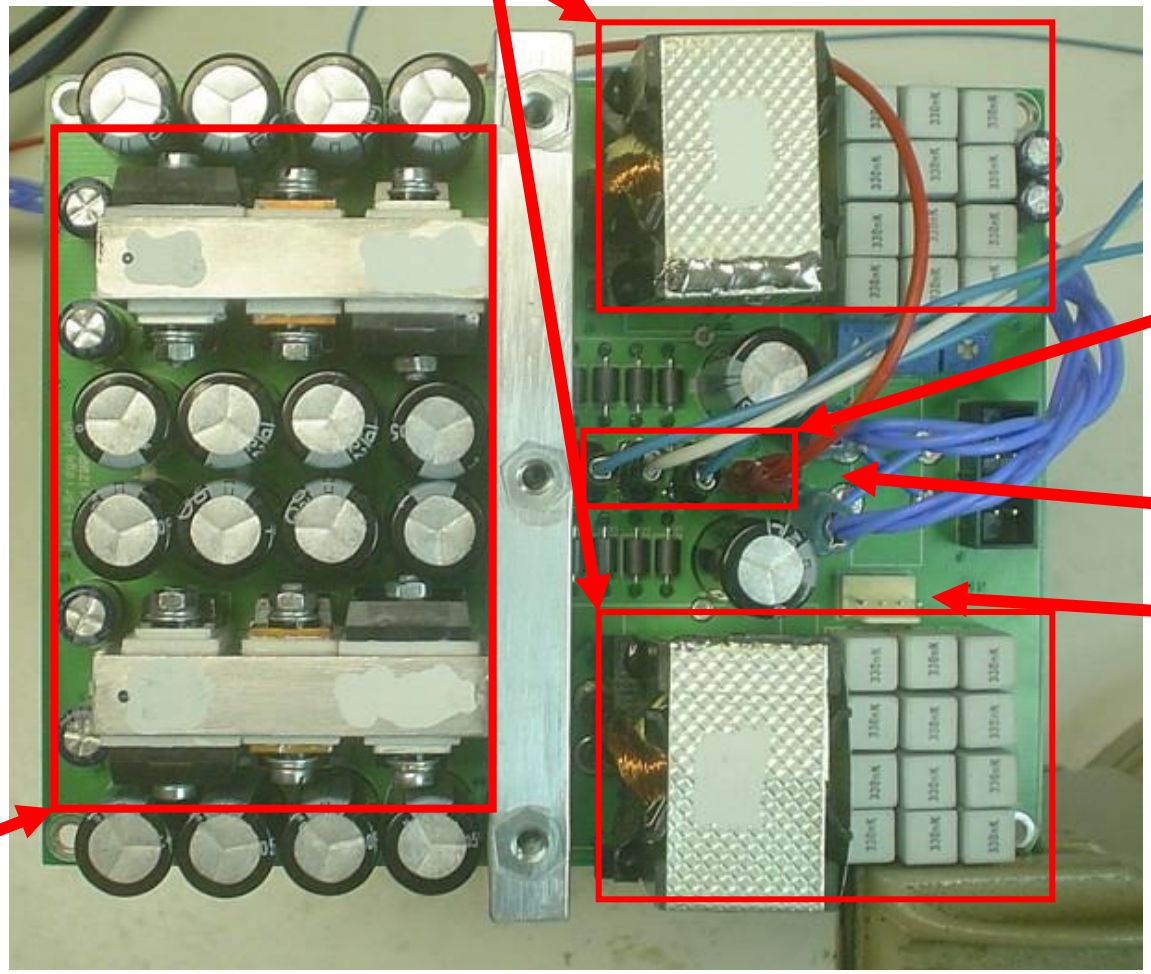
Amplifier A, differential mode

- 500mV/div. Note: relatively clean.



Class D and EMI

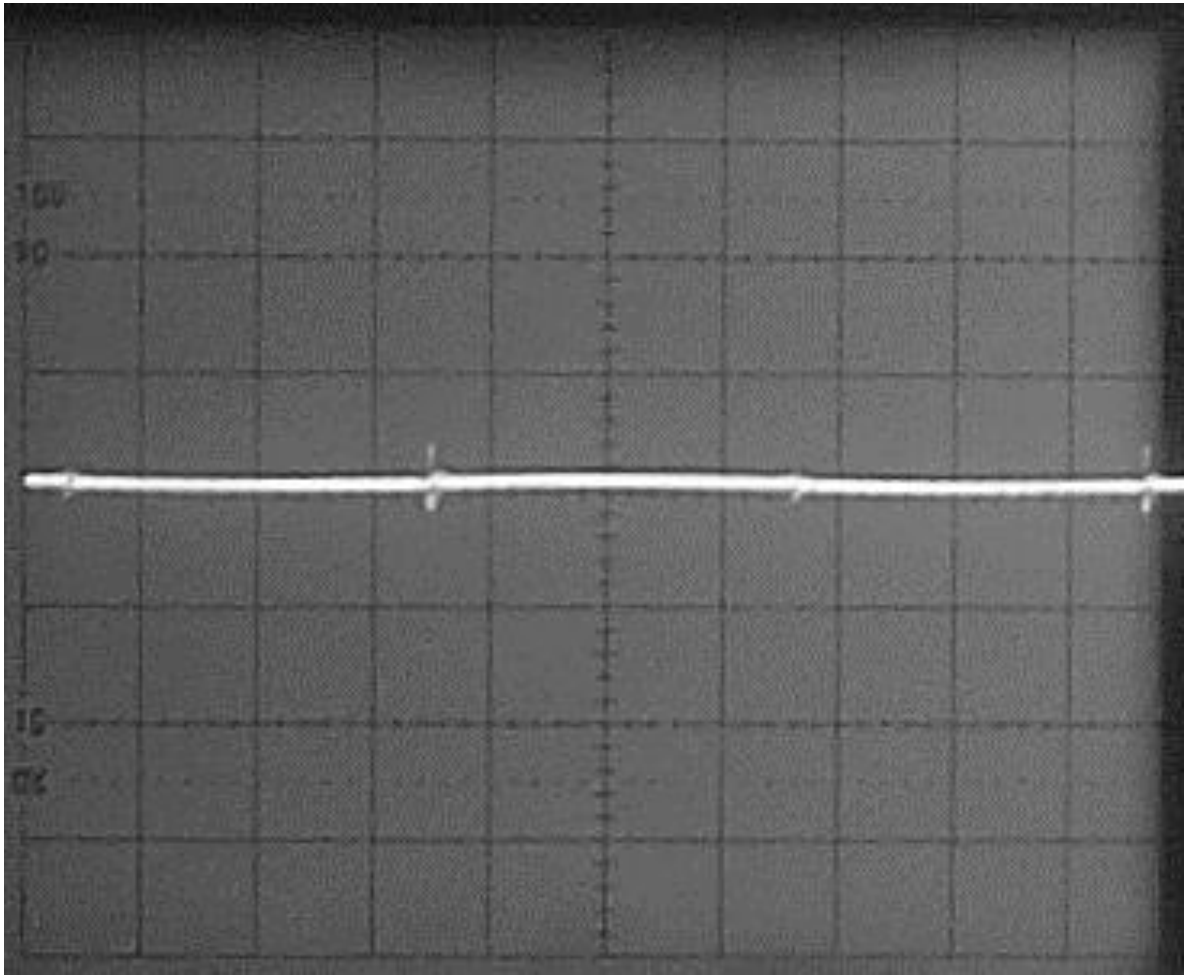
Example: Amplifier B, rated 2kW



Class D and EMI

Amplifier B, common mode

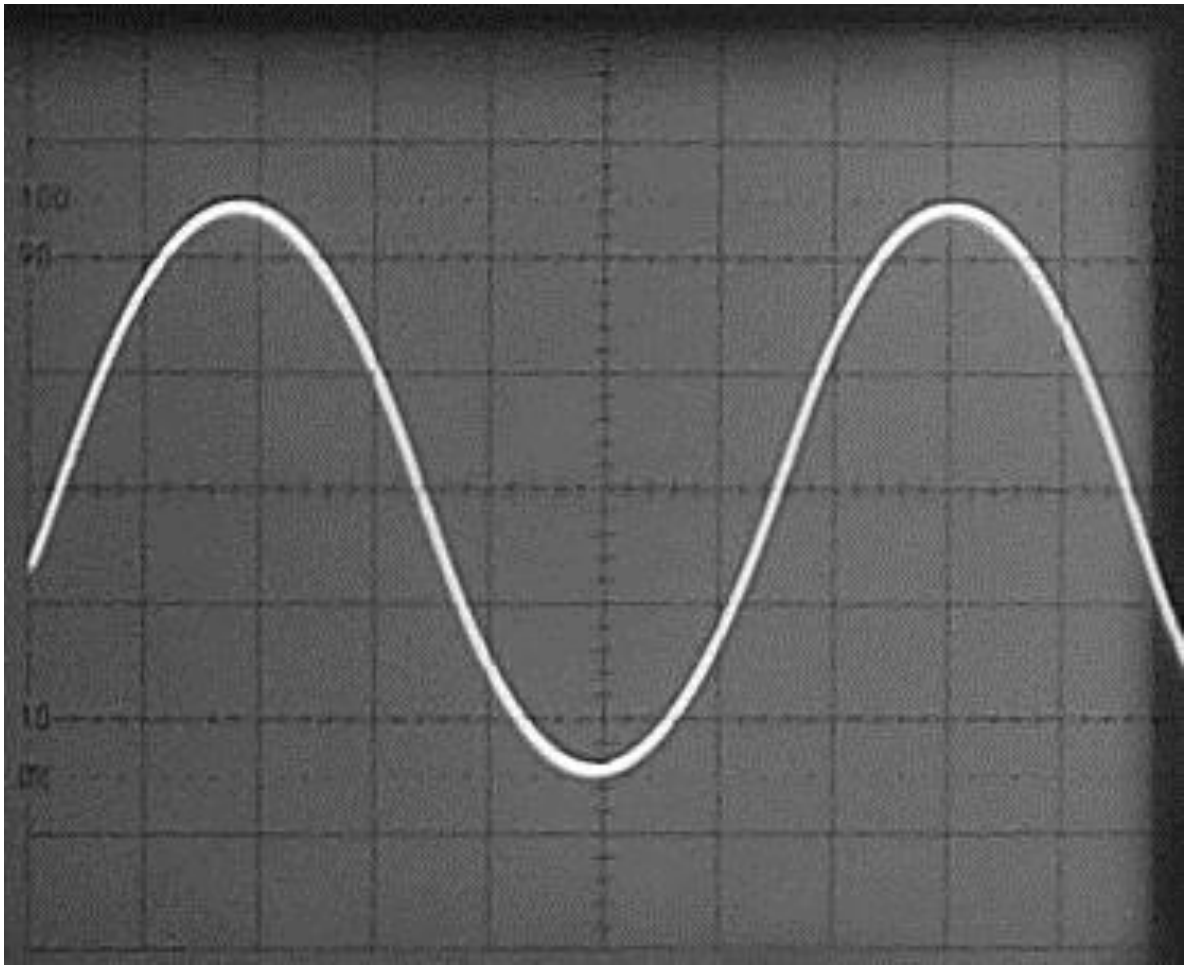
- 250mV/div. Probe clip at power GND faston tab



Class D and EMI

Amplifier B, differential mode

- 500mV/div.



Class D and EMI

Class D EMI is no mystery

- Eyeballing components and PCB gives good indication
- Invest in an analogue scope
- Don’t bother EMC testing if the scope pic isn’t squeaky clean

Summary

All “Unique Class D Technologies” are related

- All draw from a limited set of concepts
  - Modulation technique
  - Power stage arrangement
  - Loop control
- Not all are optimal
  - Too complex
  - Missed opportunities

Summary

Good design criteria: “black box”

- Audio performance
- Robustness
- Simplicity
- EMC, efficiency...

Bad design criteria: “open box”

- Perceived novelty and uniqueness
- Belief system
  - Digitalness
  - Feedbacklessness
- Powerpoint appeal

Summary of summaries

The Road To Heaven

- Specify the performance and accept the design

The Road To Hell

- Specify the design and accept the performance

Thank you!

hypex electronics